Design of Digital SoC for Operation at High Temperatures

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Failure is not an option!
Gene Kranz

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Radisav Ćojbašić,
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Abstract

There is a growing demand for Systems-on-Chip, integrating microprocessors, on-chip memories, data converters and a variety of sensors, which are capable of reliable operation at high temperatures. For instance, modern aircraft industry demands microcontrollers and electric motors to operate at high temperatures, in order to replace present hydraulic structures. This thesis explains how to design digital SoC which are capable of reliable operation at high temperatures. The essential part of this thesis focuses on the design, implementation, fabrication and high-temperature measurements of on-chip Latch based SRAM, PowerPC e200 based microcontroller, digital temperature sensor and Flash A/D converter.

Embedded on-chip SRAM modules are one of the most important components in the modern SoC. We analyze thermally-caused failures in the 6T SRAM cell and elaborate on its reliability. Further, we show that Latch based SRAM modules are preferable to 6T SRAM for reliable operation beyond 150°C, by comparing two 1 kB SRAM modules implemented in standard 0.18μm SOI CMOS process. We demonstrate reliable SRAM operation at 275°C ($f_{MAX} = 10\ MHz$, $P_{TOT} = 400\ mW$), that is by far the highest reported operating temperature for digital on-chip SRAM module.

Designing SoC for reliable operation at elevated temperatures is a significant challenge, due to increased static leakage current, reduced carrier mobility, and increased electromigration. We propose to customize a PowerPC e200 based SoC by using a dynamically reconfigurable clock frequency, exhaustive clock gating, and electromigration-resistant power distribution network. We fabricated a 20x9 mm^2 chip implementing this design in 0.35μm Bulk CMOS process. We present world's first PowerPC based SoC for reliable operation at 225°C ($f_{MAX} = 30\ MHz$, $P_{TOT} = 1.2\ W$). This design outperforms previously reported PowerPC based SoCs, which are not operational at temperatures beyond 125°C.

The on-chip measurements of the p-n junction temperature allow reliability improvements for the SoC that operates at high temperatures. Low-resolution temperature measurements are efficiently used for adjusting the optimal operation frequency and supply voltage. We used the Time-to-Digital conversion technique to design a fully-digital temperature sensor. We designed and simulated a fully-digital 5bit temperature sensor for 10°C resolution temperature measurements in between $T_{j,MIN}$ = -45°C and $T_{j,MAX}$ = 125°C. Further, using a single clock cycle Time-to-Digital conversion technique, we present a fully-digital 5bit Pulse based Flash ADC implemented in 0.18μm Bulk CMOS process. Measurement results demonstrate the state-of-the-art power efficiency result of 450 fJ/conv ($f_{MAX} = 83\ MHz$, $P_{TOT} = 900\ \mu W$).

Key words: *High Temperatures, Reliability, SoC, SRAM, Digital Temperature Sensor, Flash ADC, Time-to-Digital Conversion, Adaptive Body-Biasing, Leakage Reduction Techniques, SOI*

Résumé

La demande pour des systèmes sur puces, intégrant des microprocesseurs, des mémoires, des convertisseurs et divers capteurs, capables d'opérer de manière fiable à de hautes températures est régulièrement croissante. Par exemple, l'industrie aéronautique moderne requiert des microcontrôleurs et des moteurs électriques fonctionnant à hautes températures de manière à remplacer les structures hydrauliques existantes. Cette thèse présente une approche de conception de systèmes digitaux sur puces capables de fonctionner de manière fiable à de hautes températures. La partie essentielle de la thèse se concentre sur la conception, l'implémentation et la fabrication à haute température d'un microcontrôleur basé sur un cœur PowerPC e200, de la mémoire intégrée de type SRAM, un capteur de température digital et un convertisseur A/N de type Flash.

Les modules mémoires SRAM embarqués constituent l'un des composants les plus importants d'un système sur puces moderne. Cette thèse analyse les causes des défectuosités dues aux effets de la température dans une mémoire SRAM à cellules de 6 transistors et développe les aspects relatifs à sa fiabilité. On montre que des modules SRAM à base de latches sont préférables aux cellules à 6 transistors pour garantir des opérations fiables à des températures excédant 150°C en comparant deux modules SRAM de 1 kB réalisés avec un procédé technologique CMOS SOI 0.18μm standard. On prouve aussi la possibilité d'avoir des opérations fiables de la mémoire SRAM à 275°C ($f_{MAX} = 10\ MHz$, $P_{TOT} = 400\ mW$), ce qui est la plus haute température d'opération rapportée à ce jour pour un tel composant SRAM intégré.

La conception de systèmes sur puces fonctionnant de manière fiable à de hautes températures est un défi significatif dû aux courants de fuites statiques toujours plus importants, à la réduction de la mobilité des porteurs et aux phénomènes d'électro-migration croissants. Cette thèse propose une personnalisation du système sur puce basé sur le cœur PowerPC e200 mettant en œuvre une fréquence d'horloge reconfigurable, un contrôle exhaustif de l'activité de l'horloge (clock gating) et un réseau de distribution de l'alimentation résistant aux phénomènes d'électro-migration. Un circuit intégré de 20x9 mm^2 réalisant ces caractéristiques a été fabriqué en technologie CMOS 0.35μm standard. Cette thèse présente le premier système sur puce basé sur un cœur PowerPC spécifiquement conçu pour fonctionner à 225°C ($f_{MAX} = 30\ MHz$, $P_{TOT} = 1.2\ W$). Ce circuit offre des performances bien meilleures que celles rapportées à ce jour pour d'autres circuits similaires qui ne sont plus opérationnels au-delà d'une température de 125°C.

Des mesures de températures d'une jonction p-n ont permis d'apporter des améliorations sur le système sur puce fonctionnant à hautes températures. Des mesures de températures à basse résolution sont utilisées de manière efficace pour adapter la fréquence d'opération et la tension d'alimentation. On a utilisé une technique de conversion Time-to-Digital pour la conception d'un capteur de température numérique 5bit avec une résolution de 10°C et pour un domaine de mesure de températures entre $T_{j,MIN}$ = -45°C et $T_{j,MAX}$ = 125°C. De plus, l'utilisation d'une conversion T/D à un seule cycle d'horloge a permis de réaliser le premier convertisseur A/N Flash complètement digital au monde ne consommant que 900 μW, prouvant ainsi l'efficacité des techniques de conception basse consommation mises en œuvre.

Mots clefs : *Hautes Températures, Reliability, SoC, SRAM, Capteur de Température Numérique, Flash ADC, Conversion Time-to-Digital, Adaptive Body-Biasing, Techniques de Réduction des Courants de Fuite, SOI*

Pregled

Od nedavno postoji velika potreba za *Sistemima-na-Čipu* (SoC) koji sadrže mikroprocesore, memorije, konvertore signala, i mnoštvo različitih senzora, a koji su sposobni da rade na visokim temperaturama. Na primer, modernoj avio-industriji su potrebni mikrokontroleri i električni motori, koji funkcionišu na visokim temperaturama, da bi zamenili hidraulične delove koji se trenutno koriste. U ovoj tezi je objašnjeno kako dizajnirati digitalne SoC koji su sposobni da pouzdano funkcionišu na visokim temperaturama. Ključni deo teze se fokusira na dizajn, implementaciju, fabrikaciju i merenja na visokojim temperaturama leč SRAM memorija, mikrokontrolera koji se bazira na PowerPC e200 jezgru, digitalnog temperaturnog senzora, i Fleš A/D konvertotra.

SRAM moduli koji se nalaze na čipu su jedan od najvažnijih delova modernih SoC. Analizirali smo otkaze u 6T SRAM ćeliji koji su prouzrokovani visokim temperaturama i ispitivali smo njihovu pouzdanost. Pokazali smo da su leč SRAM moduli pouzdaniji od 6T SRAM za rad na temperaturama većim od 150°C, tako što smo uporedili dva 1 kB SRAM modula implementirana u standardnoj CMOS SOI 0.18μm tehnologiji. Demonstrirali smo pouzdano funkcionisanje SRAM modula na 275°C ($f_{MAX} = 10\ MHz$, $P_{TOT} = 400\ mW$), što je daleko najviša, do sada objavljena, radna temperatura digitalnih SRAM modula.

Dizajniranje SoC za pouzdano funkcionisanje na visokim temperaturama je ozbiljan izazov, uzimajući u obzir uvećane struje curenja, umanjenu pokretljivost nosilaca, i povišenu elektromigraciju. Predložili smo unapredjenje SoC koji se bazira na PowrePC e200 jezgru, koristeći dinamičko prilagodjavanje radne frekvencije sistema, sveobuhvatno zaustavljanje propagacije signala takta, i mrežu za distribuciju napona napajanja koja je otporna na elektromigraciju. Fabrikovali smo čip površine 20x9 mm^2, koji sadrži pomenuti dizajn, u CMOS 0.35μm tehnologiji. Predstavili smo prvi SoC, koji se bazira na PowerPC jezgru, a koji pouzdano radi na 225°C ($f_{MAX} = 30\ MHz$, $P_{TOT} = 1.2\ W$). Ovaj dizajn je po mnogim aspektima superioran u odnosu na ostale SoC koji se baziraju na PowerPC jezgu i pri tom nisu funkcionalni na temperaturama većim od 125°C.

Merenja temperature *p-n* spoja na samom čipu omogućavaju unapredjenje pouzdanosti SoC koji rade na visokim temperaturama. Temperaturna merenja niske rezolucije se efikasno koriste za podešavanje optimalne radne frekvencije i napona napajanja sistema. Iskoristili smo T/D konverziju za dizajniranje digitalnog temperaturnog senzora. Dizajnirali smo i simulirali kompletno digitalni 5bit temperaturni senzor rezolucije 10°C za merenja u opsegu od $T_{j,MIN}$ = -45°C do $T_{j,MAX}$ = 125°C. Dalje, korišćenjem T/D konverzije koja se odvija u jednom ciklusu signala takta, prezentovali smo kompletno digitalni 5bit Fleš ADC implementiran u

standardnoj CMOS 0.18μm tehnologiji. Rezultati merenja su pokazali vrhunsku efikasnost u potrošnji energije od 450 fJ/conv ($f_{MAX} = 83\ MHz$, $P_{TOT} = 900\ \mu W$).

Ključne reči: *Visoke Temperature, Pouzdanost, SoC, SRAM, Digitalni Temperaturni Senzor, Fleš ADC, T/D Konverzija, Redukovanje Struja Curenja, SOI*

Contents

List of Acronyms

- **SoC** - **S**ystem(s) **o**n **C**hip
- **IC** - **I**ntegrated **C**ircuit(s)
- **ASIC** - **A**pplication **S**pecific **I**ntegrated **C**ircuit(s)
- **SOI** - **S**ilicon **o**n **I**nsulator
- **MOSFET** - **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
- **CMOS** - **C**omplementary **MOS**
- **ABB** - **A**daptive **B**ody **B**iasing
- **Dff** - **D** **fl**ip **fl**op
- **SRAM** - **S**tatic **R**andom **A**ccess **M**emory
- **RISC** - **R**educed **I**nstruction **S**et **C**omputing
- **TDC** - **T**ime **D**igital **C**onversion
- **ADC** - **A**nalog **D**igital **C**onversion
- **FoM** - **F**igure **D**igital **C**onversion
- **ECU** - **E**ngine **C**ontrol **U**nit
- **EMA** - **E**lectro **M**echanical **A**ctuator(s)
- **AEA** - **A**ll **E**lectric **A**ircraft

List of Publications

Selected Publications

- C. Slater, R. Cojbasic, T. Maeder, Y. Leblebici, and P. Ryser. Packaging Technologies for High Temperature Control Electronics. *IMAPS Conference on High Temperature Electronics Network (HiTEN)*, July 2013, Oxford, UK.

- R. Cojbasic, O. Cogal, P. Meinerzhagen, C. Senning, C. Slater, T. Maeder, A. Burg, and Y. Leblebici. FireBird: PowerPC e200 Based SoC for High Temperature Operation. *IEEE Custom Integrated Circuits Conference (CICC)*, September 2013, San Jose, CA, USA.

In Press

- R. Cojbasic, O. Cogal, C. Slater, T. Maeder, and Y. Leblebici. FireBird: PowerPC e200 Based SoC for High Temperature Operation. *Elsevier Microelectronics Journal*, 2014.

- R. Cojbasic and Y. Leblebici. Reliability Analysis and Implementation of the SRAM for Operation at High Temperatures. *Elsevier Solid-State Electronics Journal*, 2014.

Submitted

- N. Katic, R. Cojbasic, A. Schmid and Y. Leblebici. A Sub-mW Pulse-Based 5-bit Flash ADC with a Time-Domain Fully-Digital Reference Ladder. *IEEE Transactions on VLSI*, 2014.

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1 Introduction

Nowadays, reliability is an important requirement for almost all users of integrated circuits. The challenge of realizing the required levels of reliability is increasing due to technology scaling. A simple definition of reliability is the probability that a device will not fail during its useful lifetime [1]. The ITRS (*International Technology Roadmap for Semiconductors*) emphasizes reliability as one of the most important concerns for the next generation semiconductor devices. In its most recent report from 2013 [2], the *Chapter 6* of the document refers to the reliability and highlights operation at high temperatures as on of the most important reliability challenges. Demanding application profiles, such as the operation in extreme environment, are bringing semiconductors operation at high temperatures into the focus.

1.1 Reliability in Aerospace Applications

Typically, summary of the high temperature applications includes aerospace and downhole oil industries. For the purpose of this thesis, we will focus on the aerospace industry as the major application domain. The aerospace industry established the AQEC (*Aerospace Qualified Electronic Component*) standard in 2005 [3]. This standard was jointly developed by the aerospace and semiconductor industries to define the minimum requirements for commercial off-the-shelf electronic components used in aerospace applications. A valid reliability for electronic components defined by AQEC is measured by thousands of operating hours at high temperatures, usually 100.000 hours at 225°C. Extremely high reliability requirements are a consequence of several aircraft accidents in recent history.

In September 1998, a *McDonnell Douglas MD-11* aircraft, operated by *Swiss International Airlines*, crashed into the sea off Nova Scotia following an in-flight electrical fire. Tragically, there were no survivors among 215 passengers and 14 crew members on board. Later, in September 2008, a *Boeing 757-200*, operated by *American Airlines*, lost significant electrical systems functionality en-route and landed after making a visual approach to Chicago O'Hare airport. Fortunately, none of the 192 passengers were injured and there was only minor damage to the aircraft landing gear. Finally, in August 2010, an *Airbus A321-200*, operated by

British Airways, suffered an en-route electrical malfunction while cruising over the Northern Sudan. It resulted by immediate loss of the both pilot displays an uncommanded change of a left wing flaps to low attitude. The flight crew saw that the rudder trim indicated several units from neutral although they had not made any inputs. The subsequent return of the rudder trim, which had not previously been intentionally moved, to neutral removed all abnormalities and the flight was completed without further complications. Again fortunately, none of the 49 passengers were injured.

Clearly, the modern aerospace industry desires highly reliable electronic components for the next generation aircraft. The integration of new technology into existing design and manufacturing flow requires demanding validation steps. For this purpose, Airbus provides a system integration test-bench, also known as the *Iron Bird* [4]. It is a ground-based engineering tool used to incorporate and validate vital aircraft systems, including electrical flight controls. The Iron Bird for the brand new, state-of-the-art, *A350 XWB* is presented in Fig. 1.1.

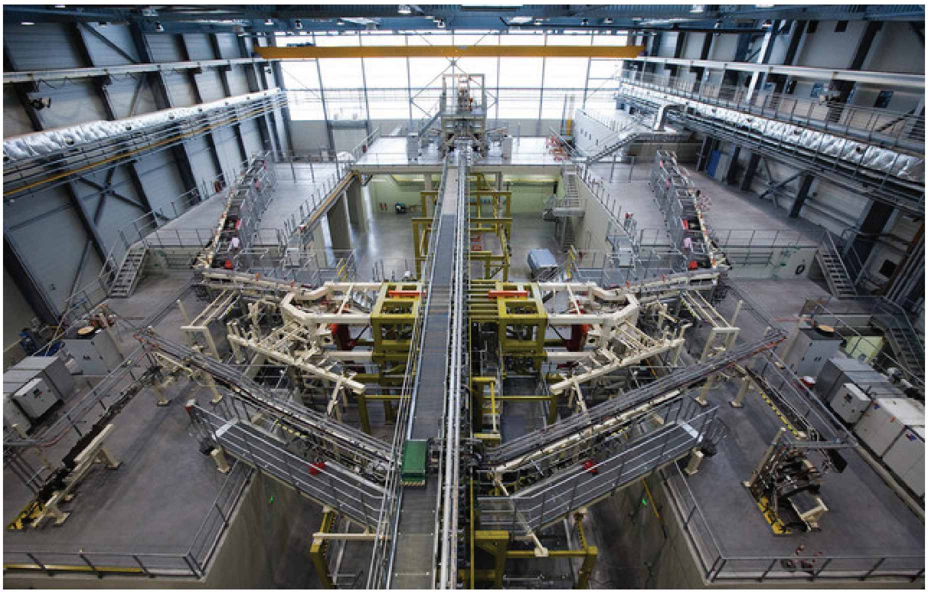


Figure 1.1: The Airbus A350 XWB Iron Bird Test-Bench.

1.2 Scope of Work

The work presented in this thesis is mainly done within the *European Commission's Seventh Framework Program, $FP7^{th}$*, CREAM (*Compact and Reliable Electronic Integrated in Actuators and Motors*) project [5] [6]. The CREAM project was initiated in 2009 by *Sagem Défense Sécurité*, a member of the *SAFRAN Group*. Until the end of the project in 2013, the *European Union* invested more than EUR 4M [7].

The CREAM project aim was to improve performance and reliability of the EMA (*Electro-Mechanical Actuators*) operating in high temperature environment. In order to address such a challenging goal, it is targeted to develop an advanced, miniaturized and reliable technological platform, including advanced electronic components and assembly methods.

Further, the compact and reliable EMA is to be used in the AEA (*All-Electric Aircraft*) concept. The AEA represents a new design concept for commercial aircraft design and manufacturing. The main novelty introduced by this concept is using only electromechanical actuators and electrical systems for powering the flight-time used surfaces (ailerons, flaps and spoilers), landing gear retraction, and air-conditioning instead of the presently used hydraulic and pneumatic structures. It is evident that reliable EMA are the most critical technological bottleneck in achieving the ambitious technological vision of AEA. The EMA technology transfer implemented during the CREAM project is presented in Fig. 1.2 [8].

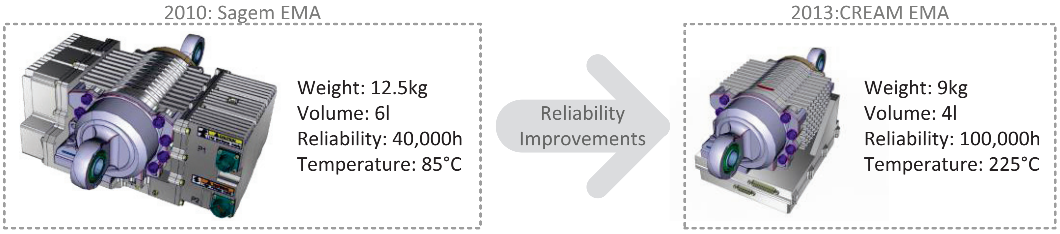


Figure 1.2: The EMA Technology Implemented During the CREAM Project.

By the CREAM specifications, novel EMA concept has to demonstrate high power density of 4 to 8 kW/kg and a compact volume of 4 l. In order to provide a compact EMA solution, the control and power electronics modules have to be placed together below the electrical motor. Such configuration exposes electronic components to the constant source of the thermal-energy, generated by the electric motor operation. As fan based cooling systems would increase the weight and complexity, all the electronic components must be capable of high temperature operation. That is why the CREAM project demands validation of electronic components reliability in high temperature environment. For aeronautics industry, standard validation requirement is to demonstrate reliable operation of at least 100.000 hours at 225°C, with integrated health monitoring functionality.

The essential part of this thesis focuses on operation principle definition, implementation and fabrication of electronic components capable of operation in high temperature environment. We report our main achievements in therms of design techniques for improving reliability. Also, we present high temperature measurement results which confirm that electronic components presented in this work could be used for the next generation EMA.

1.3 State-of-the-Art

In this thesis, we will assume that a given temperature could be considered as *high temperature* if it exceeds 125°C. The definition is taken from the NASA (*The National Aeronautics and Space Administration*) agency definition of an extreme environment [9]. According to the NASA agency definition, an environment is considered extreme if one or more of the following criteria are met:

- *Heat flux*: exceeding 1 kW/cm^2.
- *Hypervelocity impact*: higher than 20 km/s.
- *Low temperature*: lower than -55°C.
- ***High temperature***: higher than +125°C.
- *Thermal cycling*: outside of the military standard range of -55°C to +125°C.
- *High pressure*: exceeding 20 bar.
- *High radiation*: total ionizing dose exceeding 300 $krad$.

We will consider, from now on, the reliable operation at a given high temperature as the most important performance indicator. Thus, we are comparing reports on the maximum operating die temperature, Tj_{MAX}, that could be placed among the state-of-the-art achievements. In the following sections, we will present featured high temperature product lines from the main suppliers, *Honeywell International Inc.*, *Texas Instruments Inc.* and *Analog Devices Inc.*.

1.3.1 Honeywell High Temperature Products

In the late 1990s, DARPA (*Defense Advanced Research Projects Administration*) funded a consortium (*Boeing*, *Honeywell*, *Pratt and Whitney*, and *United Technologies*) to develop and demonstrate high temperature electronics for jet engine control applications [10].

Table 1.1: The Honeywell High Temperature Product Line Portfolio.

Model	Description	Tj_{MAX} [°C]
HT83C51	8051 μC	225
HT6256	32kB SRAM Memory	225
HTADC12	12bit 100kHz ADC	225
HTOP01	Op Amp	225

Honeywell introduced in 1996 a reliable and affordable processing and design methodologies for integrated circuits capable of operation from -55°C to 225°C. The initial product line included analog components, microcontrollers and memory modules [11]. The high temperature product line portfolio, including microcontrollers, data converters, analog components and memory modules, is presented in Table 1.1.

Designed to operate continuously for at least 5 years at 225°C, the high temperature product line provides signal conditioning, data acquisition, and control applications in high temperature environments. To reduce size and power consumption, Honeywell combined different high temperature components into a MCM (*Multi-Chip Module*), presented in Fig. 1.3.

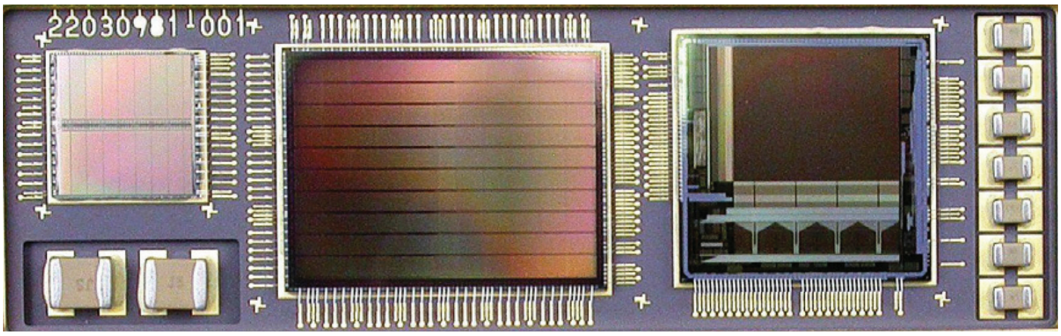


Figure 1.3: The Honeywell Multi-Chip Module.

1.3.2 Texas Instruments HiRel Products

Texas Instruments *High-Reliability Defense & Aerospace* was created in 1978 to serve the special requirements of the military customers [12]. The TI continues to expand its line of *Enhanced Products* with value-added qualifications and processing. The HiRel product line portfolio, including digital signal processors, microcontrollers, data converters, analog components and memory modules, is presented in Table 1.2.

Table 1.2: The TI HiRel Product Line Portfolio.

Model	Description	Tj_{MAX} [°C]
SM320F2812-HT	DSP	210
SM470R1B1M-HT	ARM7 μC	210
SM28VLT32-HT	4MB Flash Memory	210
ADS6142-HT	14bit 65MHz ADC	210
OPA2333-HT	Op Amp	210

In 2012, along with the increased interest in the oil in deeper wells, the TI introduced the HEAT (*Harsh Environment Acquisition Terminal*) evolution module, presented in Fig. 1.4. It was tailored for the downhole drilling application. This evolution module provides signal conditioning, data capturing, and processing in measurement applications, while drilling or logging.

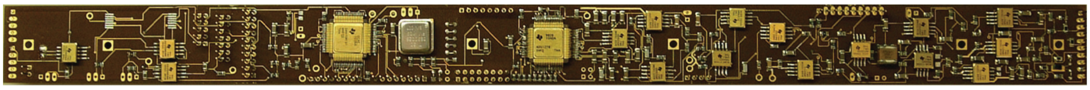


Figure 1.4: The TI HEAT Evolution Module.

1.3.3 Analog Devices High Temperature Products

In 2011, Analog Devices launched the high temperature product line for designers in oil and gas exploration [13]. Analog Devices high temperature product line portfolio, including operational and instrumentation amplifiers, voltage reference and accelerometer, is presented in Table 1.3.

Table 1.3: The AD High Temperature Product Line Portfolio.

Model	Description	Tj_{MAX} [°C]
AD8634	Operational Amp	210
AD8229	Instrumentation Amp	210
ADR225	Voltage Reference	210
ADXL206	Accelerometer	210

1.3.4 Summary

As presented in this section, there are just a few major suppliers in the high temperature electronic components market. Nevertheless, these suppliers offer wide range of components in their product lines, including microcontrollers, memories, data converters and analog components.

These product lines should be considered as the foundation stone. There are indicators that downhole oil industries will increase their orders in the near future, especially after recent discoveries of deep oil basins [14]. Thus, the mentioned suppliers are considered as pioneers in likely large market of high temperature electronic components.

The state-of-the-art products in the high temperature electronic components market will be compared to the work presented in this thesis. In the following chapters, we will present an SRAM module, microcontroller, temperature sensor and data converter, designed and implemented for the operation at high temperatures.

1.4 Contributions

This section outlines thesis contents and highlights the most important achievements, presented in:

- **Chapter 1.** This chapter brings into focus the importance of reliable operation at high temperatures. It is proving, using the aerospace industry as an example, that high reliability levels must be achieved in extreme environment applications. Further, it provides the overview of the state-of-the-art electronic components which qualified for the operation at high temperatures.

- **Chapter 2.** This chapter is dedicated to semiconductor physics at high temperatures. First, we analyze thermally-caused effects in silicon semiconductors which are causing changes in their behavior with respect to the room temperature (25°C) operation. After that, we analyze how these changes impact the MOS transistors operation at high temperatures. In parallel, we discuss how these changes of the MOS transistors behavior impact performance of the logic gates and more complex digital systems. Finally, we discuss high temperature measurement results of the stand-alone MOS transistors and CMOS inverters.

- **Chapter 3.** This chapter begins with thermally-caused failure analysis of the conventional 6T SRAM cell. Further, we introduce a novel fully-digital latch-based SRAM cell which is robust to thermally-caused failure mechanisms. Finally, we present measurement results of two 1 kB SRAM modules implemented in standard 0.18μm SOI CMOS process. We demonstrate reliable SRAM operation at 275°C ($f_{MAX} = 10\ MHz$, $P_{TOT} = 400\ mW$), that is by far the highest reported operating temperature for fully-digital on-chip SRAM module.

- **Chapter 4.** In this chapter we present the Firebird, the first PowerPC e200 based SoC for operation at high temperatures. First, we introduce the PowerPC e200 core, on-chip memory modules, bus system and peripherals architecture. Further, design decisions and implementation trade-offs are presented. Finally, we present fabricated 20x9 mm^2 chip implementing this design in 0.35μm Bulk CMOS process. Measurement results demonstrate reliable operation at 225°C ($f_{MAX} = 30\ MHz$, $P_{TOT} = 1.2\ W$).

- **Chapter 5.** This chapter is dedicated to the T/D conversion design technique and its high temperature applications. First, we introduce this time-domain technique and reveal its strong points. After that, we exploit it for designing a Digital Temperature Sensor and a Flash ADC. We present simulation results of a fully-digital 5bit temperature sensor for 10°C resolution temperature measurements in between $T_{j,MIN}$ = -45°C and $T_{j,MAX}$ = 125°C. Finally, we present a fully-digital 5bit Pulse based Flash ADC implemented in 0.18μm Bulk CMOS process. Measurement results demonstrate the state-of-the-art power efficiency result of 450 fJ/conv ($f_{MAX} = 83\ MHz$, $P_{TOT} = 900\ \mu W$).

- **Chapter 6.** In this chapter we present the custom measurement and test techniques which are used for high temperature experiments. We introduce a novel micro-heater based thermally-controlled test-bench capable of reaching 250°C.

- **Chapter 7.** This chapter concludes the thesis and gives directions for the future work.

2 Semiconductor Physics at High Temperatures

This chapter is dedicated to the semiconductors physics at high temperatures. First, we analyze thermally-caused effects in silicon semiconductors which are causing changes in their behavior with respect to the room temperature (25°C) operation. After that, we analyze how these changes impact the MOS transistors operation at high temperatures. In parallel, we discuss how these changes in MOS transistors impact performance of the logic gates and more complex digital systems. Finally, we discuss measurement results and conclude this chapter.

2.1 Introduction

This chapter focuses on the semiconductor physics at high temperatures. This theoretical and experimental study is a foundation stone for work presented in the following chapters. Taking into account its importance, we will discuss into details on how temperature impacts semiconductors properties, and what could be learned from the theory and used for the future design implementations.

The ITRS (*International Technology Roadmap for Semiconductors*) emphasizes reliability as one of the most important concerns for the next generation semiconductor devices. In its most recent report from 2013 [2], the *Chapter 6* of the document refers to the reliability and highlights operation at high temperatures as on of the most important reliability challenges. Demanding application profiles, such as the operation in extreme environment, are bringing semiconductors operation at high temperatures into the focus.

The fundamental limitation of silicon semiconductors operation at high temperatures is their band gap of 1.10 eV. Once a semiconductor is exposed to sufficiently high thermal energy, it allows the thermal excitation of electrons into conduction band. By doing so, once semiconductor, it becomes fully conductive and useless as an electronic device.

That is why it is important to observe other semiconductors which have larger band gap and that could eventually be used for the high temperature applications.

2.1.1 The Wide Band Gap Semiconductors

The two main representatives of wide band gap semiconductors, which could be used for the high temperature applications [15], are 6H SiC (*Silicon-Carbide*) and 2H GaN (*Gallium-Nitride*) with band gaps of 3.05 eV [16] and 3.40 eV [17], respectively.

As presented in [18] for the SiC process, a continued improvement in fabrication techniques and wafer substrates are required for profitable production. It has been further explained in [19] that the SiC process is favoring the NMOS transistors disabling preferable CMOS design technique. Also, there are still many uncertainties related to process materials quality, reliability, and packaging techniques [20].

The GaN process and its applications are presented in [21]. It has been recently reported in [22] that there is a significant progress in development of GaN substrates, what is a key step in further commercialization and reducing fabrication costs. However, there are serious reliability issues which are to be solved [23] before this process becomes eligible for wider acceptance.

Taking into account already mentioned facts, the SiC and GaN processes are not mature enough for high volume production. It could not be expected that the wide band gap semiconductor devices will find a lot of the applications until the ambient temperature exceeds 300°C, having that commercially available CMOS Bulk and SOI processes are already satisfying requirements for digital VLSI systems at room temperature operation (25°C). In this work we demonstrate that for the applications operating in range of 25°C to 300°C, the commercially available CMOS Bulk and SOI processes are highly competitive to the wide band gap semiconductors. The advantages of using the CMOS Bulk and SOI processes are numerous and we emphasize their compatibility with the typical design-flow (Spice transistor models, design, simulation and layout tools) as the most important. Thus, this work focuses on the silicon semiconductors operating at high temperatures.

2.2 Silicon Physics at High Temperatures

Deep understanding of silicon semiconductors behavior requires analysis of several important parameters at elevated temperatures. We will analyze those parameters which are seriously affected by thermal energy and significantly impact MOS transistor performance. Our analysis will start with the thermally-caused intrinsic carriers generation, carriers mobility and the threshold voltage.

The following section correlates this theoretical study with the measurements of the static leakage and drain currents. We provide integral theoretical analysis and experimental results for all MOS transistor parameters that are affected by thermal energy.

An NMOS transistor fabricated in the 0.18 μm SOI process is presented in Fig. 2.1. This microphotograph is courtesy of *IBM Corporation* [24].

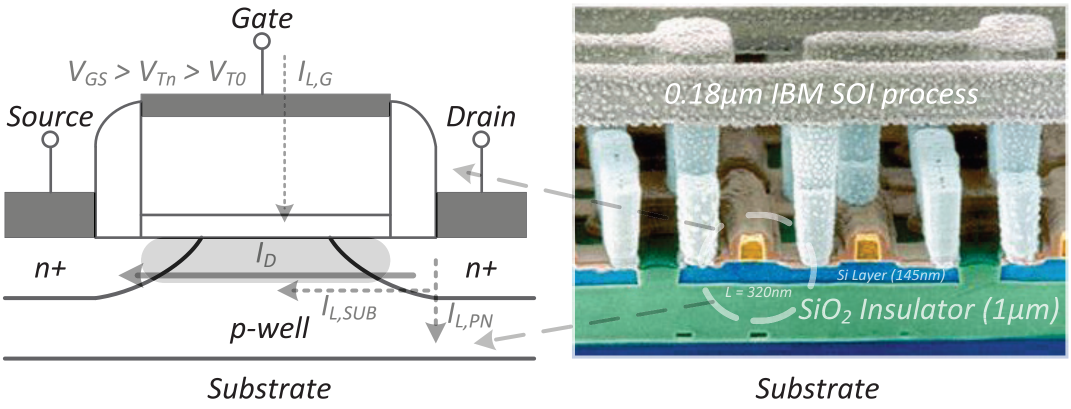


Figure 2.1: An NMOS Transistor Fabricated in the SOI Process.

2.2.1 Intrinsic Carriers Generation

The intrinsic carriers thermal generation is fundamental physical limitation for operation of semiconductors at high temperatures. The concentrations of thermally generated intrinsic carries are exponentially dependent of temperature [25]:

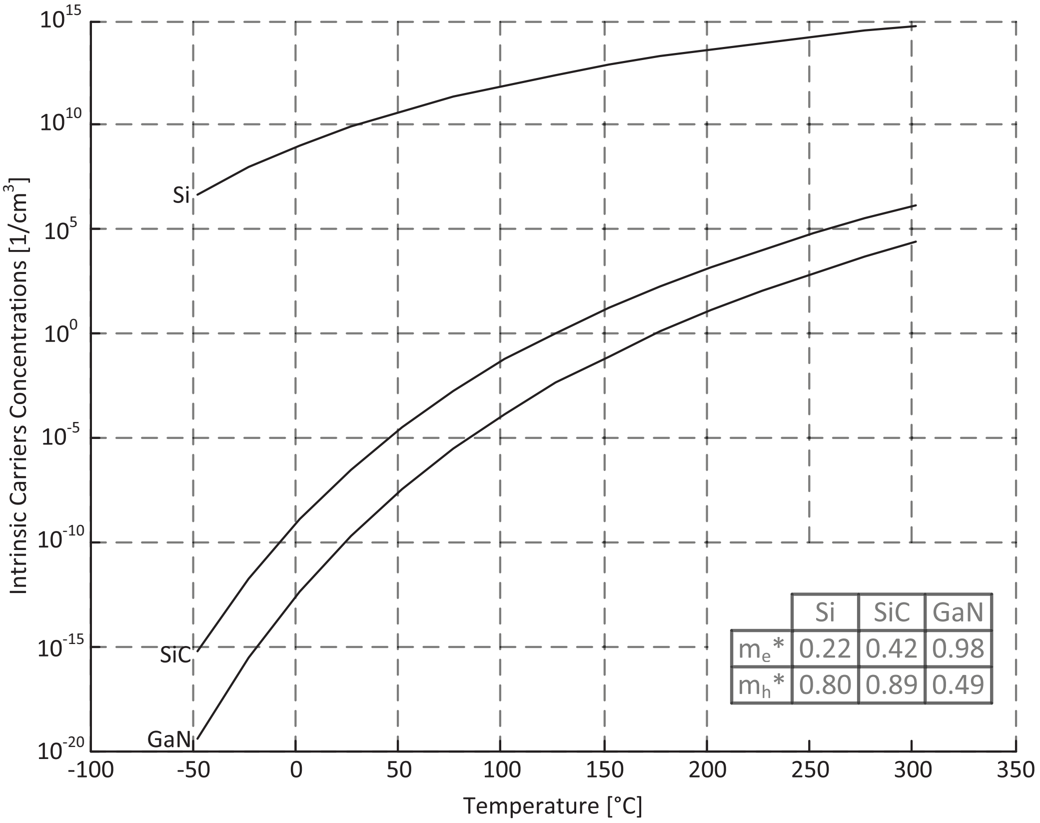
$$n_i = 4.9 \times 10^{15} \times \left(\frac{m_e^\star m_h^\star}{m_0^2} \right)^{0.75} \times T^{1.5} exp \left(-\frac{E_g}{2kT} \right) \tag{2.1}$$

where T is the p-n junction temperature, $m_e^\star$ and $m_h^\star$ are the effective mass for electrons and holes, respectively, E_g is energy band gap and k is Boltzmann's constant.

It is very important to compare intrinsic carriers concentrations of silicon with previously mentioned wide band gap semiconductors, the SiC and GaN. The effective mass for electrons and holes, $m_e^\star$ and $m_h^\star$, have been previously reported in: [26] for silicon, [27] and [28] for SiC, and in [29] and [30] for GaN. Comparison of the intrinsic carriers concentrations for silicon, SiC and GaN, is presented in Fig. 2.2.

The wide band gap semiconductors need larger quantities thermal energy to generate significant concentrations of intrinsic carriers. In case of silicon for the temperature of 250°C, the intrinsic carriers concentration of $10^{15}\ 1/cm^3$ becomes comparable to donors and acceptors doping levels. As it could be observed in Fig. 2.2, high concentration levels are achieved at much higher temperatures for SiC and GaN. This result indisputably confirms that wide band gap semiconductor devices will be used in future for the high temperature applications.

To analyze further thermally-caused intrinsic carriers generation in silicon, we compared it with the doping concentrations. The n- and p-*type* doping concentrations, $N_D \approx 10^{17}\ 1/cm^3$ and $N_A \approx 10^{18}\ 1/cm^3$, are provided by the 0.18 μm SOI process supplier. For the given process, the intrinsic carriers concentrations become harmful beyond 250°C. Equalization of intrinsic carriers concentrations and doping levels degrades device performance by decreasing both the majority carriers mobility and the threshold voltage.



	Si	SiC	GaN
m_e^*	0.22	0.42	0.98
m_h^*	0.80	0.89	0.49

Figure 2.2: Comparison of the Intrinsic Carriers Concentrations.

More importantly, it further results by exponentially increased static leakage and linearly decreased drain currents. We will explain this effect more into details in the following sections.

2.2.2 Carriers Mobility

The ability of carriers to move through the silicon crystal lattice is reduced at elevated temperatures. This thermally-caused effect occurs when atoms in the crystal lattice have more thermal vibrational energy which results by more frequent collisions with the carriers moving through the crystal. The resulting decrease in carrier mobility at elevated temperatures is explained by the phonon scattering in [31], [32] and [33]. The majority carriers mobilities temperature dependence is described by the Caughey-Thomas experimental equation [34]:

$$\mu_T = \mu_0 \times \left(\frac{T}{300K}\right)^{2.5} \tag{2.2}$$

Carrier mobility temperature dependence is presented in Fig. 2.3. We are using low-field mobilities of $\mu_e = 407.64\, cm^2/Vs$ and $\mu_h = 86.27\, cm^2/Vs$, provided by the SOI 0.18 μm process supplier. It could be observed that mobility degrades exponentially for both holes and electrons. Thus, thermally-caused phonon scattering equally affects *n*- and *p-type* carriers transport in silicon semiconductors.

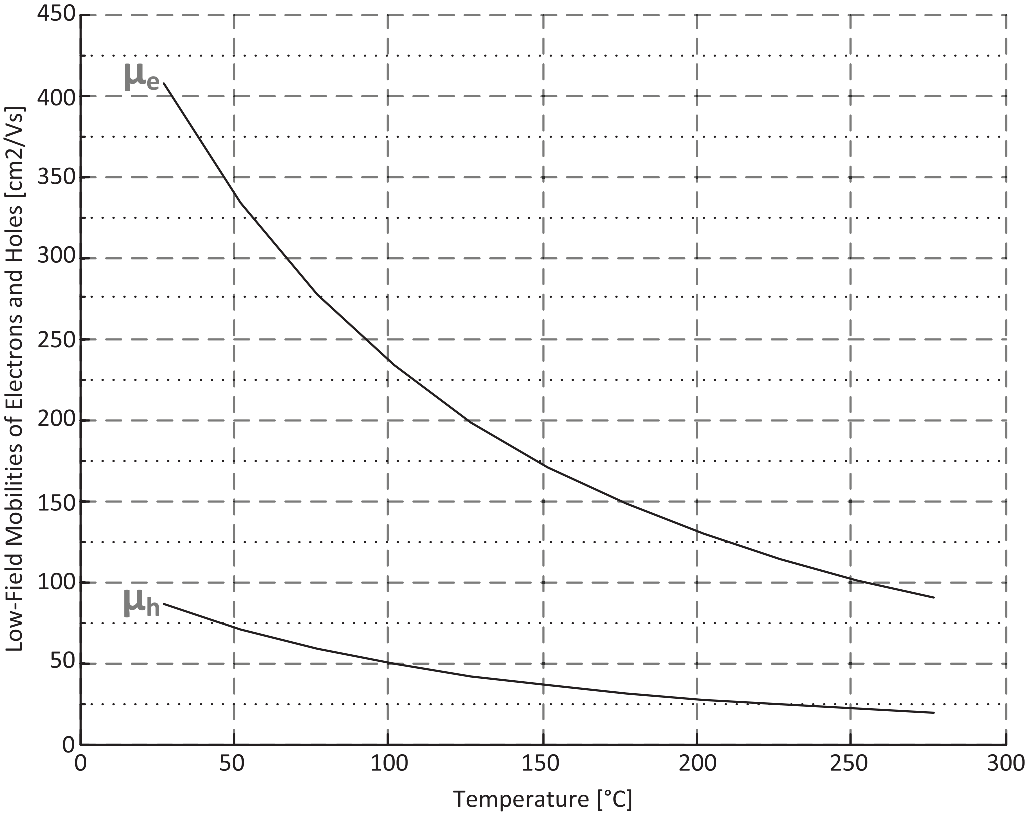


Figure 2.3: Majority Carriers Mobilities at High Temperatures.

To conclude, decreased carriers mobility reduces the amount of drain current that a MOS transistor conducts when operating at high temperatures.

2.2.3 The Threshold Voltage

The threshold voltage of an NMOS transistor, V_{Tn}, could be described by the Shichman-Hodges equations [35]. This model takes into account the body-effect and is determined by the following equation:

$$V_{Tn} = V_{T0} + \gamma \left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|} \right) \tag{2.3}$$

where V_{SB} is the source-to-body substrate bias and the V_{T0} is threshold voltage for the zero substrate bias. The process-dependent body-effect parameter, γ, is defined by following equation:

$$\gamma = (t_{ox}/\epsilon_{ox}) \sqrt{2q\epsilon_{Si} N_A} \tag{2.4}$$

where t_{ox} is oxide thickness, ϵ_{ox} is the gate oxide permittivity, ϵ_{Si} is the permittivity of silicon, N_A is the *p-type* doping concentration, and q is the elementary charge.

Most important factor of the threshold voltage equation is the Fermi surface potential ϕ_F, which is defined by the following equation:

$$\phi_F = V_t \ln \frac{N_A}{N_i} \tag{2.5}$$

where N_A is doping concentration for the *p-type* silicon and N_i is thermally generated intrinsic carriers concentration. The thermal voltage, V_t, is defined by the following equation:

$$V_t = \frac{kT}{q} \tag{2.6}$$

where k is Boltzmann's constant and q is elementary charge. The thermal voltage is approximately equal to $V_t \approx 26\,\mathrm{mV}$ at the room temperature. The threshold voltage dependence of high temperatures for the SOI CMOS 0.18 μm process is presented in Fig. 2.4.

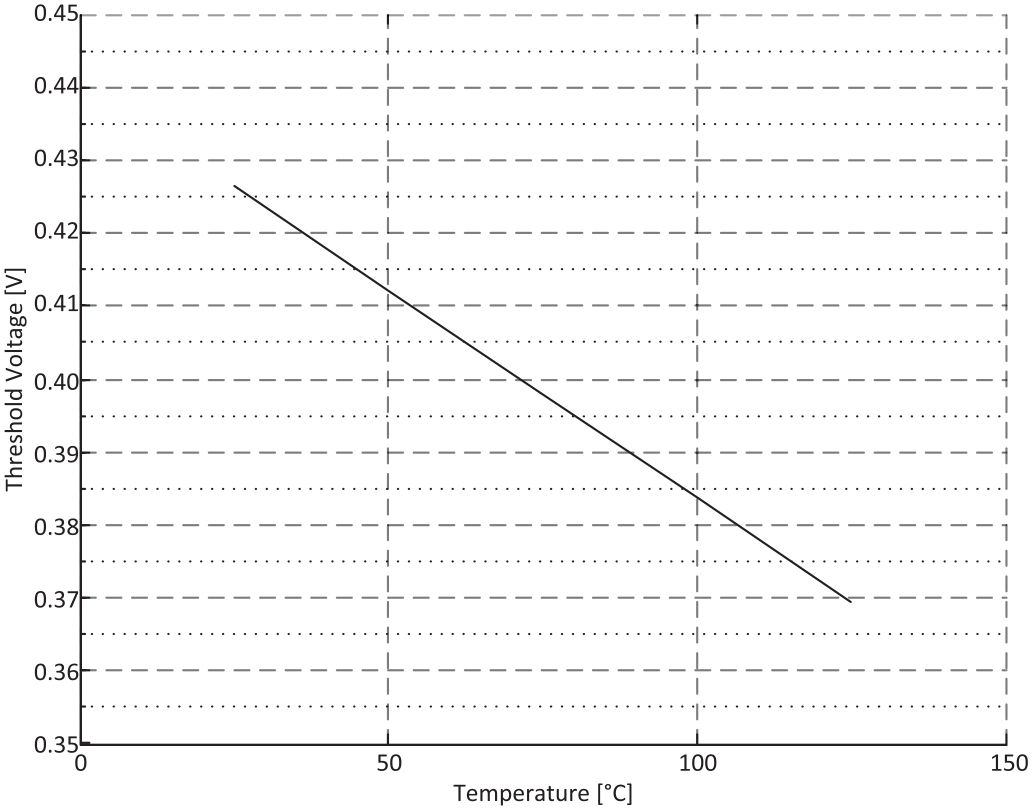


Figure 2.4: The Threshold Voltages at High Temperatures.

If we follow equations in the reverse order, the thermal voltage V_t is directly proportional to temperature. Further, the Fermi surface potential ϕ_F is directly proportional to thermal voltage V_t and it also linearly increases with elevated temperatures. Finally, the threshold voltage V_{Tn} is directly proportional to the Fermi surface potentials ϕ_F.

It could be observed that the threshold voltage decreases linearly with increased temperatures. From physical prospective, this means that less voltage in needed on the *Gate* with respect to the *Substrate* to form conduction channel. Further, from electrical prospective, it results by earlier conduction of an NMOS transistor at elevated temperatures. This essentially means that for the same amount of voltage across *Gate* and *Source*, V_{GS}, a MOS transistor starts to conduct current earlier at high temperatures.

2.3 Measurement Results

In order to verify thermal energy impact on the silicon operation, we measured basic electronics devices, diodes and MOS transistors. Several experiments are conducted on test devices fabricated in 0.18 μm SOI and 0.35 μm Bulk processes.

2.3.1 Diode Currents at High Temperatures

The diode current, I_{AC}, which passes through a diode when associated voltage V_{AC} is applied across *Anode* and *Cathode*, is approximated by the following equation:

$$I_{AC} = I_S \times exp\left(\frac{V_{AC}}{nV_t}\right) \tag{2.7}$$

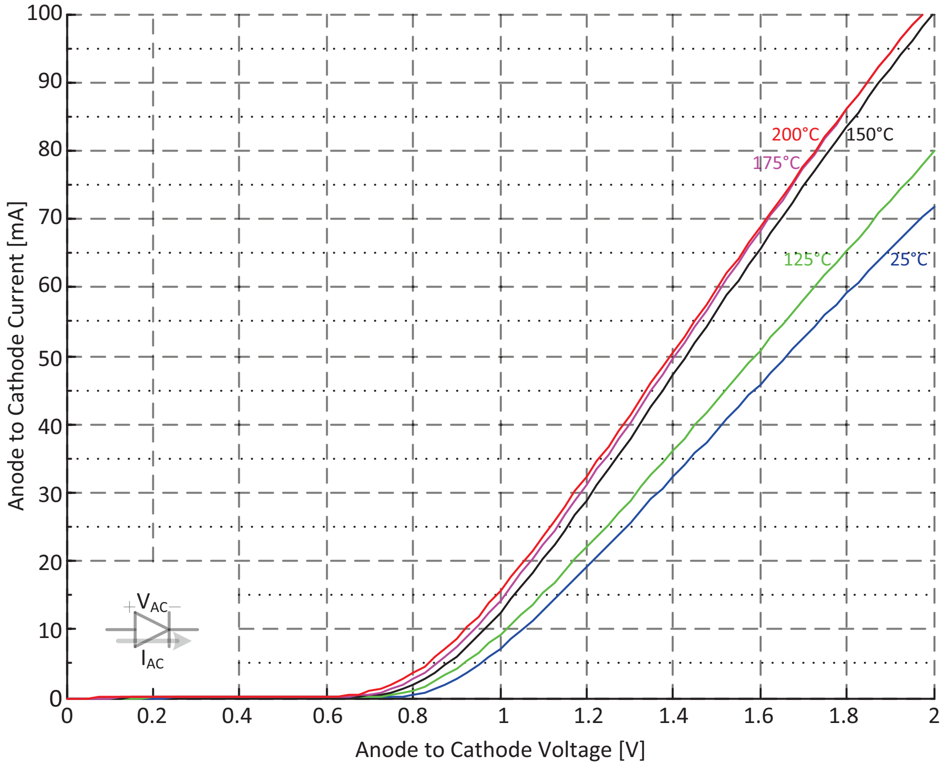


Figure 2.5: The Diode I-V Characteristics at High Temperatures.

where I_S is the reverse bias saturation current ($I_S \approx 50\,\text{fA}$), V_t is the thermal voltage ($V_t \approx 26\,\text{mV}$ at the room temperature), and n is ideality factor which represents an empirical and process-dependent constant ($n \approx 1$). All the mentioned values and constants are valid for the Bulk CMOS 0.35 μm process. The $I - V$ characteristics of a diode operating at high temperatures is presented in Fig. 2.5.

It could be observed that elevated temperatures result by earlier conduction of a diode. This essentially means that for the same amount of voltage across *Anode* and *Cathode*, V_{AC}, a diode starts to conduct current earlier at high temperatures.

Also, the reason for I-V characteristics non-ideality is explained by a serial resistance, R_S, of the depletion region. It could be observed that this serial resistance, R_S, is decreased at elevated temperatures. Such measurement results could be correlated with increased conductivity at elevated temperatures, as it is explained in [36].

2.3.2 Drain Current of MOS Transistor at High Temperatures

The drain current, I_D, of an NMOS transistor operating in the saturation region, could be approximated by the following Shichman-Hodges equation [35]:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{Tn})^2 \tag{2.8}$$

where μ_e is the low-field mobility for electrons, W is the *Gate* width, L is the *Gate* length, and C_{ox} is the *Gate* oxide capacitance.

It is very important to analyze how temperature affects the drain current I_D of an NMOS transistor that operates in the saturation region. Starting with the threshold voltage V_{Tn} that decreases linearly with temperature, we may conclude that for the constant voltage V_{GS}, the overdrive voltage $(V_{GS} - V_{Tn})^2$ increases by the power of two. On the other side of the equation, the carriers mobility μ_e decreases exponentially with temperature. Taking into account that the other factors in the drain current I_D equation are thermally-stable, we may conclude that the drain current I_D decreases linearly with increased temperatures.

We fabricated and measured *n-* and *p-type* MOS transistors in the Bulk 0.35 μm and SOI 0.18 μm processes. The summary of device properties is presented in Table 2.1. High temperature $I_D - V_{DS}$ characteristics of SOI MOS transistors is presented in Fig. 2.6.

Table 2.1: The MOS Transistors Properties.

Type	Process	W [μm]	L [μm]
NMOS	0.18 μm SOI CMOS	1.5	0.32
PMOS	0.18 μm SOI CMOS	6	0.32
NMOS	0.35 μm Bulk CMOS	4	0.35
PMOS	0.35 μm Bulk CMOS	8	0.35

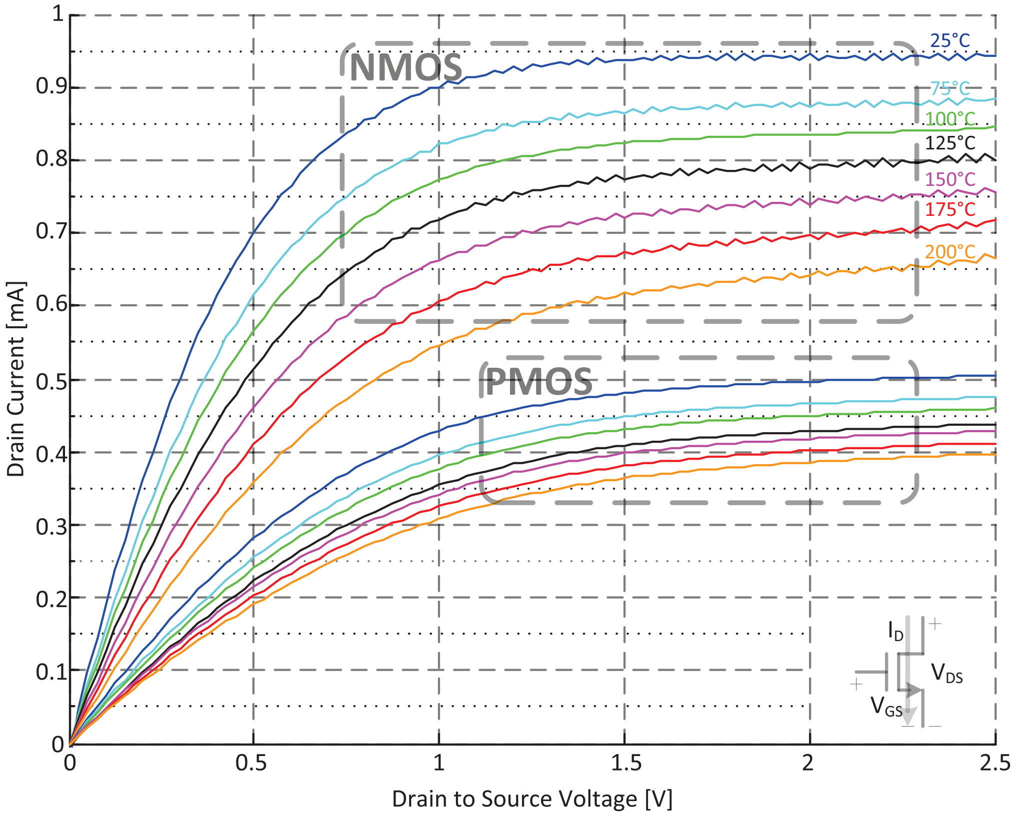


Figure 2.6: The SOI MOS Transistors I-V Characteristics at High Temperatures.

Table 2.2: The Drain Current Derating Factors.

Process	0.35 μm Bulk	0.35 μm Bulk	0.18 μm SOI	0.18 μm SOI
Type	NMOS	PMOS	NMOS	PMOS
W/L	5	20	10	20
$I_{D,25°C}$ - $I_{D,75°C}$ $[\mu A]$	25.40	11.64	56.44	29.34
$DF_{25°C-75°C}$ [%]	1.85	1.04	5.99	5.82
$I_{D,75°C}$ - $I_{D,100°C}$ $[\mu A]$	52.00	24.98	40.36	15.88
$DF_{75°C-100°C}$ [%]	3.86	2.25	4.56	3.34
$I_{D,100°C}$ - $I_{D,125°C}$ $[\mu A]$	48.20	22.94	44.26	21.32
$DF_{100°C-125°C}$ [%]	3.73	2.11	5.24	4.64
$I_{D,125°C}$ - $I_{D,150°C}$ $[\mu A]$	46.40	22.18	45.98	9.50
$DF_{125°C-150°C}$ [%]	3.73	2.09	5.74	2.17
$I_{D,150°C}$ - $I_{D,175°C}$ $[\mu A]$	45.00	19.98	37.50	16.18
$DF_{150°C-175°C}$ [%]	3.75	1.92	4.97	3.78
$I_{D,175°C}$ - $I_{D,200°C}$ $[\mu A]$	42.86	19.02	53.16	15.14
$DF_{175°C-200°C}$ [%]	3.71	1.86	7.41	3.67

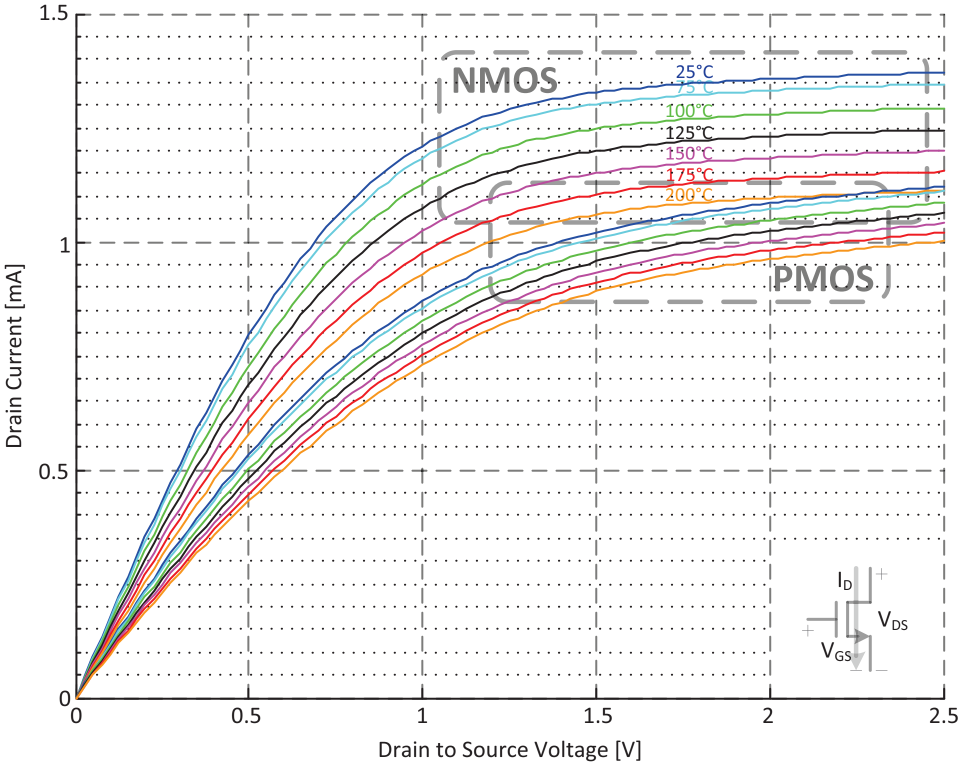


Figure 2.7: The Bulk MOS Transistors I-V Characteristics at High Temperatures.

High temperature $I_D - V_{DS}$ characteristics of Bulk MOS transistors is presented in Fig. 2.7.

It could be observed in the measurement results that drain current I_D linearly decreases with increased temperature. The maximum operating frequency of CMOS logic gates is affected by reduced drain currents and it results by increased gate propagation delays at high temperatures. This result strongly verifies previous theoretical analysis.

We advance in analysis of the measurement results by quantifying impact of thermal energy to the drain current. The main idea is to determine the derating factors (DF) for drain currents degradation with respect to temperature [37]. Results of this analysis are presented in Table 2.2.

The drain current derating coefficients, DF, show identical behavior of both the n- and p-*type* MOS transistors fabricated in both the SOI and Bulk processes. Once the die temperature goes beyond 100°C, the DF keep almost constant values:

- For the 0.35 μm Bulk process, the DF are approximately 4 % and 2 %, for the NMOS and PMOS, respectively.

- For the 0.18 μm SOI process, the DF are approximately 5 % and 3.5 %, for the NMOS and PMOS, respectively.

The DF could be used later when estimating the CMOS logic gate propagation delays at elevated temperatures, having that it mostly depend on the drain current.

2.3.3 Static Leakage Current of MOS Transistor at High Temperatures

We are particularly interested in static leakage current a MOS transistor. As already presented in Fig. 2.1, we identify different static leakage currents which occur in a MOS transistor [38]:

• The Tunneling Gate Oxide leakage current, $I_{L,G}$, occurs with reducing the *Gate* oxide thickness and increasing the electric field across the oxide. This results by the tunneling of electrons from *Substrate* to *Gate*. However, this component of the total static leakage current is negligible with the respect to the following two components.

• The Reverse-Bias leakage current, $I_{L,PN}$, occurs when the *Drain* and *Source* to well junctions are reversely biased, causing the *p-n* junction leakage current.

• The Sub-threshold leakage current, $I_{L,SUB}$, occurs when the voltage across *Gate* and *Source* is below the threshold voltage V_{Tn}. When in the weak inversion, the MOS transistor channel conducts leakage current from *Drain* to *Source*.

For reverse-bias *Gate* to *Source* voltages (in CMOS, equivalent to the non-conductive state of a MOS transistor) and *p-type* doping, the total static leakage current ($I_{L,PN} + I_{L,SUB}$) could be approximated by the following equation [15]:

$$I_L = -q \times A \times n_i \times \left(\frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right) \tag{2.9}$$

where q is the elementary charge, A is the area of the *p-n* junction throughout which the static leakage current is generated, N_D is the *n-type* doping concentration, W is the width of the junction depletion region, D_P is the hole diffusion constant, and τ is the effective minority carrier lifetime. It is obvious that the static leakage current, I_L, depends on the intrinsic carriers concentration, n_i, by the power of two. To conclude, the static leakage currents increase exponentially with increased temperature.

We measured the static leakage current of the same MOS transistors presented in the previous section. The high temperature measurement results are presented in Fig. 2.8. It could be observed that, for both the 0.18 μm SOI and 0.35 μm Bulk processes, the static leakage current exponentially increases with increased temperature. This result strongly verifies previous theoretical analysis.

The *n-* and *p-type* MOS transistors fabricated in the SOI process leak less current comparing to the Bulk devices. The SOI process is inherently robust to the substrate leakage currents, due to the buried oxide layer (SiO_2) which insulates MOS transistor wells from the substrate. Having that the substrate leakage currents are important component of the static leakage, its absence significantly reduces total static leakage current. On top of that, MOS transistor wells are separated by the STI (*Shallow Trench Isolation*), which prevents well-to-well leakage. Such SOI process property additionally reduces total static leakage current.

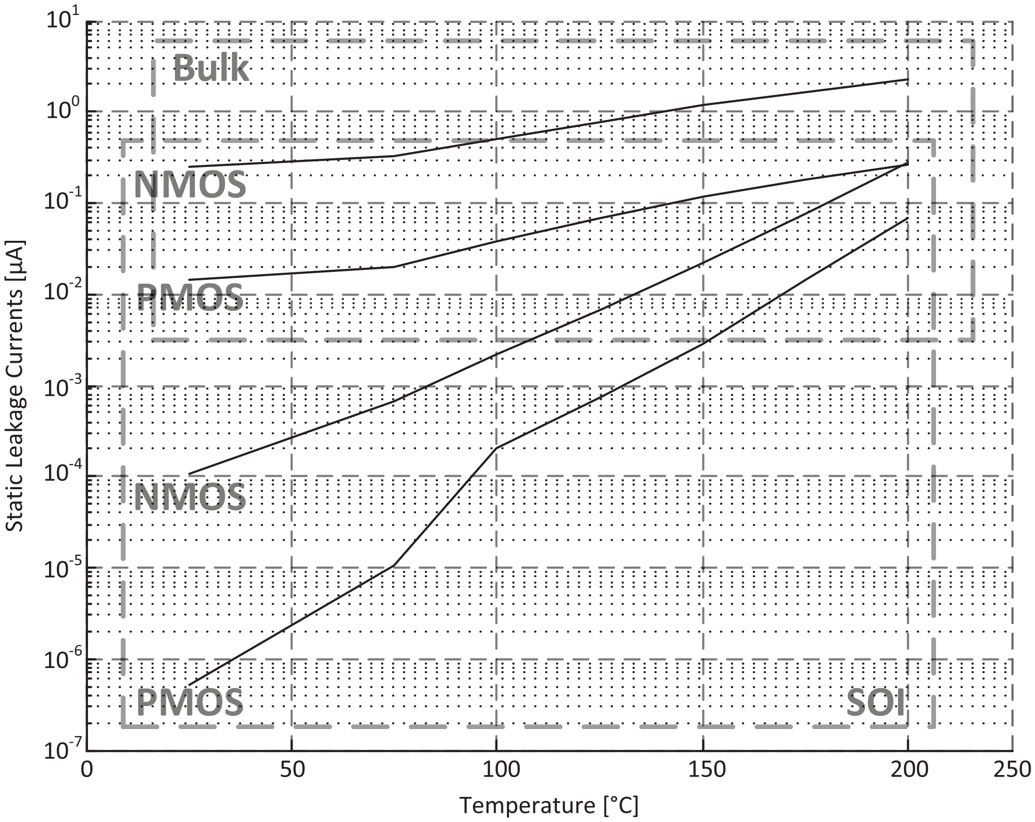


Figure 2.8: Static Leakage Currents at High Temperatures.

Taking it all into account, the SOI process is the right choice for applications which desire low leakage currents in MOS transistors. A typical example of such applications are found in operation at high temperatures.

The static leakage currents, I_L, are harmful for the CMOS logic gates operation. By its construction, the CMOS (*Complementary MOS*) design technique and logic gates implemented in it, operate using exclusively its n- or *p-type* networks, so never both of them at the same time. This prevents CMOS logic gates to consume any static power, having that there could not be any direct path in between the power supply rails (VDD and GND). The thermally-caused leakage currents create direct paths in between the power supply rails and initiate static power consumption which presence is highly undesirable in the CMOS logic gates.

Not just that this static power contributes to the total power consumption and silicon self-heating, but is also reduces the driving strength of a CMOS logic gates. The reason for this also lies in the complementary nature of the CMOS design technique. A CMOS logic gate drives a following consecutive logic gate or gates by either the n- or *p-type* network. One of these two networks contains a direct path from the power supply rails (GND for the n-*type* and VDD for the *p-type*) to the logic gate output and drives the following consecutive logic gate by drain currents of the MOS transistors which are found in the path.

When there in no leakage current, the MOS transistors drain currents drive by its full strength the following CMOS logic gate. In case when the thermally-caused leakage currents exponentially increase at elevated temperatures, their conduction deviate certain amount of the drain current and the CMOS logic gate driving strength is reduced. Increased static leakage currents cause driving strength issues which increase the propagation delay, but also seriously reduces reliability of a CMOS logic gate. Once static leakage currents become comparable to the drain current of a MOS transistor, a CMOS logic gate cannot drive following logic gates any more.

To conclude, the static leakage currents are highly undesirable in the CMOS logic gates. They reduce the driving strength and increase propagation delays. More important then that is their negative impact on the reliability of a CMOS logic gate.

2.4 Comparison of the SOI and Bulk Processes

The driving strength could be used to determine if a MOS transistor, which operates at elevated temperatures, is robust to the thermally-caused effects in silicon. The driving strength could be simply quantified as the ratio of the drain current, I_D, and the static leakage currents, I_L, for a given MOS transistor.

The MOS transistors driving strengths at high temperatures is presented in Fig. 2.9.

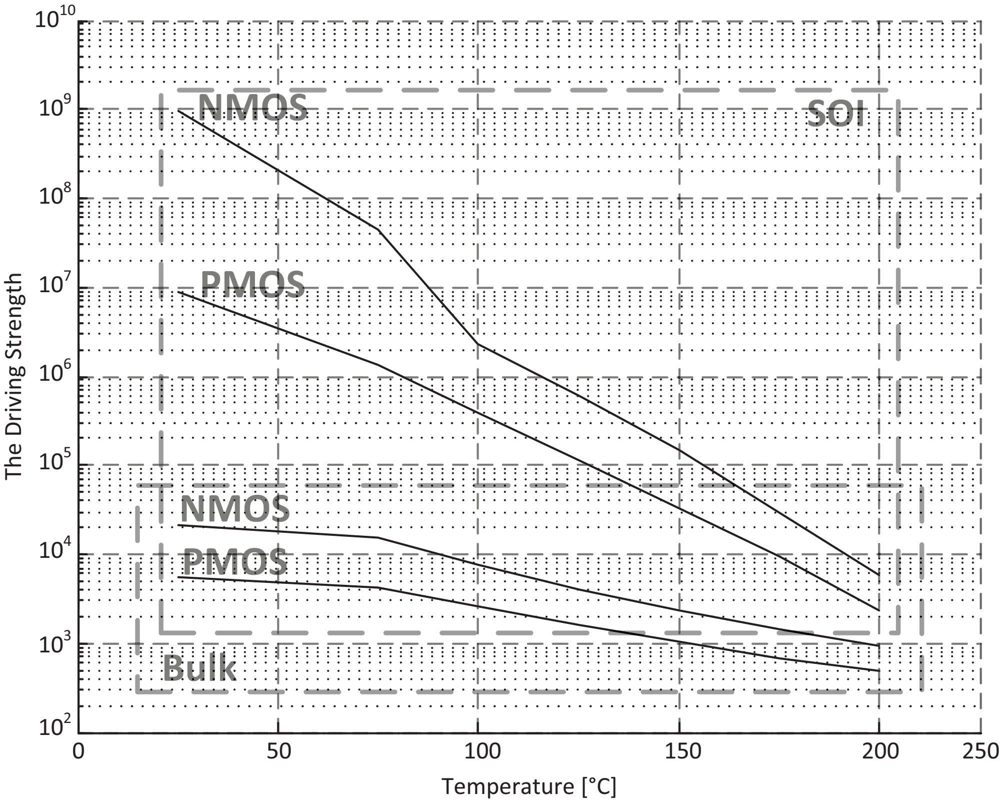


Figure 2.9: The MOS Transistors Driving Strengths at High Temperatures.

If a MOS transistor demonstrates high driving strength, that essentially means that its drain current is capable to resist to the static leakage current. Taking into account that at elevated temperatures, the drain current linearly decreases and the static leakage currents exponentially increase, the MOS transistors which have high driving strength are able to preserve performance at high temperatures. That is why the MOS transistor driving strength is considered as the most important indicator performance and reliability for the operation at high temperatures.

It could be observed that the MOS transistors fabricated in the SOI process demonstrate higher driving strength comparing to those fabricated in the Bulk process. Based on it, we may conclude that an SOI process is preferable choice comparing to the Bulk process. This conclusion does not eliminate usage of the Bulk processes for the high temperature applications. If MOS transistors, fabricated in a Bulk process, demonstrate high driving strengths, the Bulk process is eligible to be used in the high temperature applications.

2.5 The CMOS Inverter Operation at High Temperatures

Once we conducted theoretical study of thermally-caused effects in the MOS transistor, we may advance to the basic CMOS logic gates. We will observe static and dynamic properties of an CMOS inverter and analyze its behavior at elevated temperatures. The test-bench configuration is presented in Fig. 2.10.

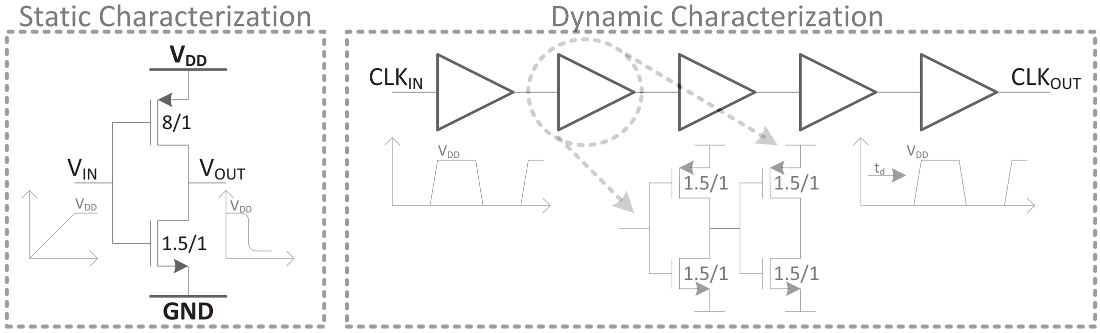


Figure 2.10: The Test-Bench for Static and Dynamic Characterization.

2.5.1 Static Behavior

We analyzed behavior of an CMOS inverter implemented in the 0.18 μm SOI process. The NMOS transistor is sized by $W/L = 1.5$, and the PMOS transistor is sized by $W/L = 8$. The input voltage, V_{IN}, takes voltages in between 0 V and 1.8 V. The CMOS inverter static characteristics are presented in Fig. 2.11.

As it can be observed, higher temperatures initiate earlier conduction. This behavior of an CMOS inverter can be explained by decreased threshold voltages at high temperatures.

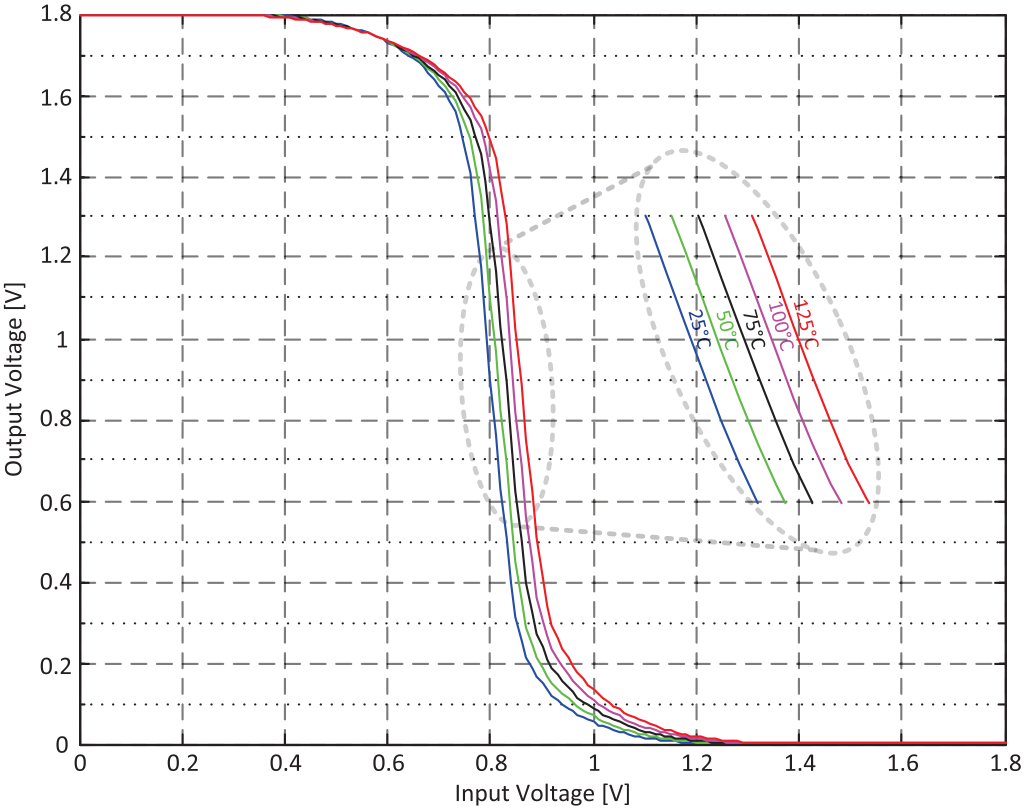


Figure 2.11: The CMOS Inverter Static Characteristics at High Temperatures.

Further, the switching of operation in between the PMOS and NMOS is shifted to higher input voltages. This means that higher input voltage is needed to completely turn-off a MOS transistor. This behavior is also a product of decreased threshold voltage, having that more reverse-bias voltage is needed to cut-off the channel of a MOS transistor.

Static characteristic of an CMOS inverter demonstrates reliable operation at high temperatures. The thermally-caused threshold voltage changes do not affect operation, and we may conclude that the CMOS design technique preserves static characteristics at elevated temperatures.

2.5.2 Dynamic Behavior

We analyzed behavior of ten CMOS inverters coupled into a simple inverter chain, implemented in the $0.18\,\mu m$ SOI process. Both the NMOS and PMOS transistors are sized by $W/L = 1.5$. The inverter chain delays a clock signal, where the clock period is 10 ns. The CMOS inverter dynamic characteristics are presented in Fig. 2.11.

The propagation delay increases with increased temperature, due to increased static leakage and decreased drain currents. As for the case of the drain current, we can also define the derating factors DF for the propagation delays.

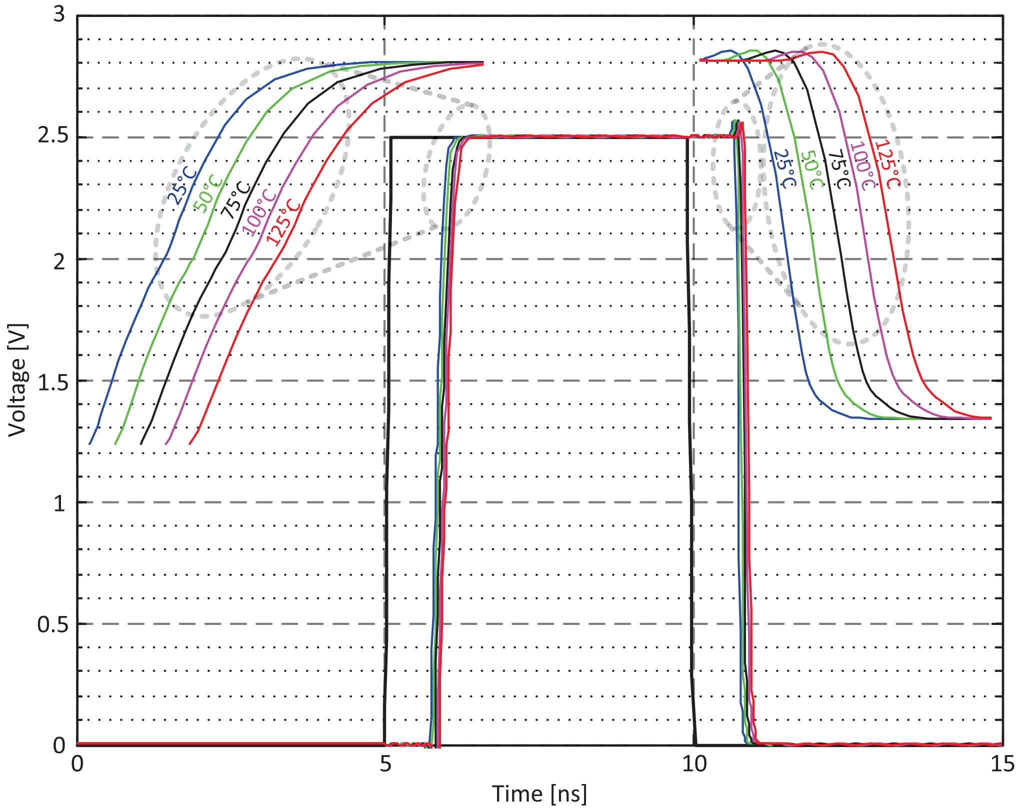


Figure 2.12: The CMOS Inverter Dynamic Characteristics at High Temperatures.

The CMOS inverter propagation delay derating factors are presented in Table 2.3. For the CMOS inverter, the propagation delay derating coefficients, DF, show identical behavior of both the n- and *p-type* MOS transistors. The DF keep almost constant values, where the DF are approximately 0.45 % and 0.70 %, for the NMOS and PMOS, respectively.

Table 2.3: The CMOS Inverter Propagation Delay Derating Factors.

CLK Transition	Rising edge	Falling edge
Operating Transistor	PMOS	NMOS
$CLK_{OUT,50°C}$ - $CLK_{OUT,25°C}$ $[ps]$	43.30	54.29
$DF_{50°C-25°C}$ [%]	0.74	0.50
$CLK_{OUT,75°C}$ - $CLK_{OUT,50°C}$ $[ps]$	41.94	47.61
$DF_{75°C-50°C}$ [%]	0.71	0.44
$CLK_{OUT,100°C}$ - $CLK_{OUT,75°C}$ $[ps]$	42.49	43.53
$DF_{100°C-75°C}$ [%]	0.71	0.40
$CLK_{OUT,125°C}$ - $CLK_{OUT,100°C}$ $[ps]$	35.50	41.85
$DF_{125°C-100°C}$ [%]	0.59	0.38

The dynamic properties of the CMOS inverter are valid for the more complex CMOS logic gates. At elevated temperatures, their performance degrades following the same trend as described by the derating factors. Further, increased propagation delays lead to reduced maximum operating frequency of more complex digital systems, as presented in the following chapters.

2.6 Conclusion

In this chapter, we presented a detailed theoretical semiconductors physics study and supported it by the experimental results. This study has significant importance for future design integrations, having that it takes a MOS transistor characteristics and applies them to CMOS logic gates and more complex digital systems. As such, this physics study is a foundation stone for the design of digital SoC which are used in the high temperature applications.

This is an integral study which takes into account both the SOI and Bulk process behaviors at high temperatures. We proved by measurements that the SOI are a preferable choice with respect to Bulk processes.

3 Latch Based SRAM Module and its Operation at High Temperatures

This chapter is dedicated to thermally-caused failures analysis of the conventional 6T SRAM cells and to the design of fully-digital latch based SRAM modules for operation at high temperatures. First, we explain our motivation to analyze failure mechanisms in the conventional 6T SRAM cell and what could be learned from the failures nature. After that, we describe a fully-digital latch based SRAM cell which is robust to thermally-caused failure mechanisms at elevated temperatures. Finally, we discuss measurement results and conclude this chapter.

3.1 Introduction

The SOI (*Silicon On Insulator*) thin-film fully or partially depleted devices significantly outclass their bulk competitors for room temperature (25°C) applications such as high-speed or low-power digital ICs [39]. The SOI technology performance is also attractive for many other niche applications, in parallel to the mainstream.

Currently, one of the most prominent field of use is high temperature applications [40]. There is a growing demand for reliable ICs integrating one or more microprocessors, on-chip memories, and a variety of sensors and actuators on a single chip that is capable to operate at high temperatures. For example, modern aircraft industry demands ICs and electric motors to operate at high temperatures in order to replace hydraulics [8]. Fully-integrated solutions allow better reliability than presently used hydraulic structures which exploit many interconnects, plugs and complex mounting procedures [41].

It has been shown in [25] that SOI technology can fulfill requirements of such applications. Thanks to well-known properties such as the absence of thermally-activated latch-up, reduced leakage currents, small threshold voltage variations with temperature and constant device output conductance, SOI technology is nowadays considered as the best contender for high temperature ICs [42]. Bulk technology hardly maintains the functionality beyond 200°C, except ones with dedicated circuit design and process customizations in order to avoid high leakage current, thermally-caused latch-up and threshold voltage shifts [42].

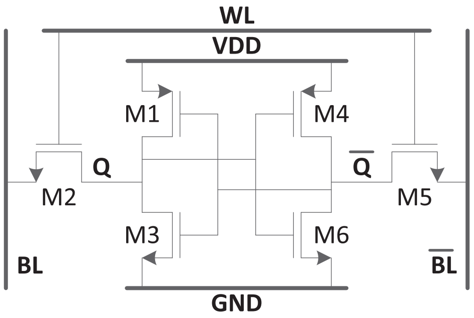
As presented in [43], on-chip SRAM modules are one of the most important components in the modern high-performance SoCs designed to operate at high temperatures and there is a strong market demand for such products. In 1996, Honeywell introduced its *High Temperature Electronics* products line which is targeting aerospace applications. They presented world's first 32 kB SRAM module for operation at 225°C. Later in 2012, Texas Instruments introduced *High-Reliability Components for Extreme Environments* products line which is mainly targeting oil-drilling applications. They presented world's first 32 MB Flash memory module for operation at 210°C. Finally in 2013, Tony Kim *et Al.* presented 8 kB 8-T SRAM module for operation at 300°C [44]. Table 3.1 compares the features and performance of the best commercial SRAM modules with this work. The maximum operating temperature, Tj_{MAX}, frequency, f_{MAX}, and total power consumption, P_{TOT}, of the aforementioned products, are taken from product datasheets.

Table 3.1: SRAM Modules for Operation at High Temperatures.

Manufacturer	Honeywell	Texas Instruments	Tony Kim *et Al.*	EPFL
Process	SOI	-	1μm SOI	0.18μm SOI
SRAM Topology	-	Flash	8T	D latch
Tj_{MAX} [°C]	225	210	300	225
f_{MAX} $[MHz]$	20	12	1	15
P_{TOT} $[mW]$	100	-	1	200
Memory Size $[kB]$	32	32000	8	1

3.2 Conventional 6T SRAM cell

As shown in Fig. 3.1, a 6T (*6-Transistor*) SRAM cell consists of a pair of inverters (M1, M3, M4, M6) coupled in a positive feedback loop creating a bi-stable circuit. This allows us storing complementary values in the Q and $\overline{Q}$ nodes. By driving the bit-lines, BL and $\overline{BL}$, high/low (low/high) and strobing the word-line, WL, a successful write operation (Write access) is completed. Prior to a read operation (Read access), the BL and $\overline{BL}$ are pre-charged to supply voltage, VDD, and the WL is enabled immediately after that allowing the pass-transistors (M2, M5) to drive BL and $\overline{BL}$ with the respect to the value that is held inside the 6T SRAM cell.



Transistor	Type	Body Contact	W[nm]	L[nm]
M1, M4	PMOS	YES	500	420
M2, M5	NMOS	NOT	500	420
M3, M6	NMOS	YES	800	420

Figure 3.1: Conventional 6T SRAM Cell.

Read and Write accesses waveforms are presented in Fig. 3.2. Depending on the access type, BL and $\overline{BL}$ are used both by the 6T SRAM cell and the line drivers. During a Write access, the BL and $\overline{BL}$ voltages are driven by the line drivers and pass transistors of the 6T SRAM cell drive nodes Q and $\overline{Q}$ with the respect to the BL and $\overline{BL}$ voltage levels.

On the other hand, during the Read access, line drivers are in the High-Z state and the 6T SRAM cell through the pass transistors drive the voltage levels of the BL and $\overline{BL}$. Usually, neighboring 6T SRAM cells share the same BL and $\overline{BL}$, WL and Sense amplifiers which are used for the differential readout.

• The read/write control signal, $RDWRT$, causes a Read access when held high or a Write access when held low. The clock signal, CLK, samples it on the falling-edge, deciding which type of the access is to be performed. The address port, $ADDR[9..0]$, defines the addressing range of the SRAM module.

• The bit write control signal, $BW[7..0]$, and data input port, $D_{IN}[7..0]$, must be stable before the clock signal initiates an access to the array. The bit write control signals, $BW[7..0]$, are active high and one signal is required for each data input bit, allowing their masking. If the signal is held high, the corresponding data input bit is written into the array cell. Otherwise, if the pin is held low, the corresponding data input bit is ignored and the array cell retains its previous content. The bit write control signals, $BW[7..0]$, and data input port, $D_{IN}[7..0]$, are non-inverting and perform no logical function during a read memory access.

• The data output port, $D_{OUT}[7..0]$, is non-inverting and not affected by a write memory access. The results of a read memory access are registered at the output and remain the same until the next read cycle.

Interface definition and related signal timings are described in Fig. 3.2.

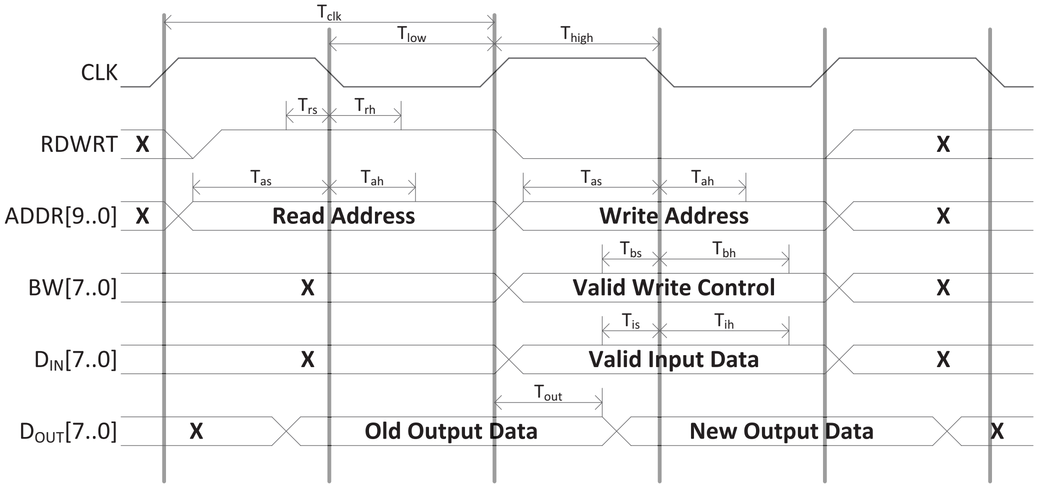


Figure 3.2: Typical Interface Definition and Signal Timings of an SRAM Module.

Default 6T SRAM interface definition and related signal timings for standard 0.18 μm SOI CMOS process are presented in Table 3.2.

Table 3.2: Default 6T SRAM Module Signal Timings for 0.18μm SOI Process.

Signal Name	Input/Output	Setup Time [ns]	Hold Time [ns]
$RDWRT$	Input	0.4	0.9
$ADDR$	Input	4.2	1.0
BW	Input	0.2	2.4
D_{IN}	Input	0.2	2.4
D_{OUT}	Output	-	6.3

3.3 Analysis of Thermally-Caused Failures in 6T SRAM Cell

Random variations, reduction of the supply voltage and elevated temperature result with different failures mechanisms in 6T SRAM cells. Such failures are generally categorized as Read and Write failures. We define four different failure types, two per Read and Write accesses:

• Write '0' (W0) failure: if the 6T SRAM cell is not capable of performing a Write access that is supposed to write a '0' into the cell, such scenario is categorized as a Write '0' (W0) failure. Thus, internal nodes Q and $\overline{Q}$ do not hold proper values of '0' and '1' respectively. Example: after performing a Write '0' access, the Q = '1' and $\overline{Q}$ = '0'.

• Write '1' (W1) failure: if the 6T SRAM cell is not capable of performing a Write access that is supposed to write a '1' into the cell, such scenario is categorized as a Write '1' (W1) failure. Thus, internal nodes Q and $\overline{Q}$ do not hold proper values of '1' and '0' respectively. Example: after performing a Write '1' access, the Q = '0' and $\overline{Q}$ = '1'.

• Read '0' (R0) failure: if the 6T SRAM cell is not capable of performing a Read access that is supposed to readout a '0' value that the cell holds, such scenario is categorized as a Read '0' (R0) failure. Thus, the cell is not capable of pulling down and up nodes BL and $\overline{BL}$, respectively. Example: after performing a Read '0' access, the BL is on higher voltage than the $\overline{BL}$.

• Read '1' (R1) failure: if the 6T SRAM cell is not capable of performing a Read access that is supposed to readout a '1' value that the cell holds, such scenario is categorized as a Read '1' (R1) failure. Thus, the cell is not capable of pulling up and down nodes BL and $\overline{BL}$, respectively. Example: after performing a Read '1' access, the BL is on lower voltage than the $\overline{BL}$.

After defining the failures types (W0, W1, R0 and R1), we designed an automated simulation environment that is used to run Monte-Carlo simulations performing Write and Read accesses by the following repetitive sequence:

$$W0 - R0 - R0 - W1 - R1 - R1 \tag{3.1}$$

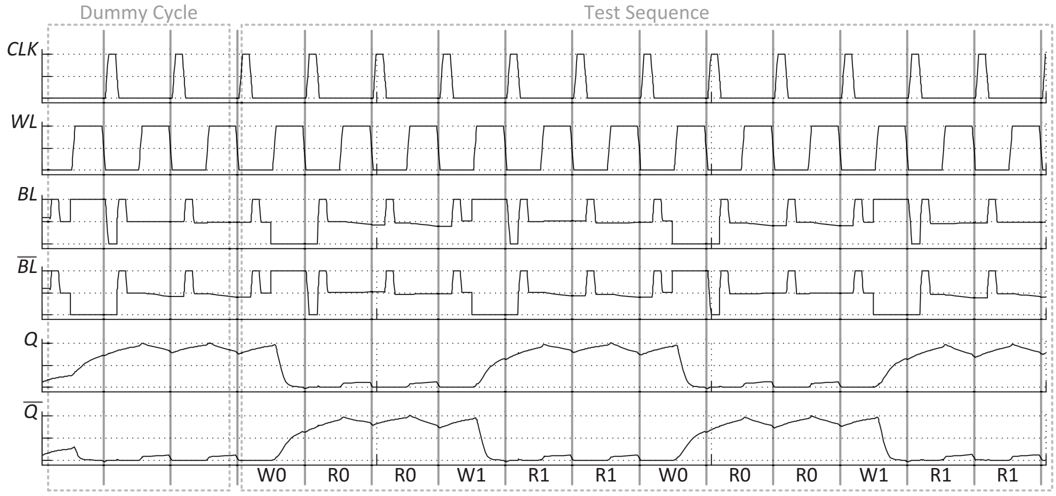


Figure 3.3: Write and Read Accesses Repetitive Test Sequence.

The sequence is designed such that all the four failure types could be easily observed. The sequence is presented in Fig. 3.3 and it is taken directly from the simulation environment.The simulation environment provides simulations for the supply voltages sweep from nominal 1.8 V to minimal 0.3 V, having step of 50 mV. For the each value of the supply voltage, we ran simulations at five different temperatures of 25°C to 125°C, having step of 25°C. Finally, for the each set of voltages and temperatures, we ran 3737 Monte-Carlo simulations, accessing the 6T SRAM cell in the sequence presented earlier.

3.3.1 Simulation of the 6T SRAM Cell Failure Rates

The simulation environment performs transient Monte-Carlo Spice simulations, where only the transistors of the 6T SRAM cell are using the technology parameters (models). The rest of the test-bench including word and bit line drivers and column sense amplifiers is implemented in *VerilogA* and it is robust to temperature and supply voltage variations. This allows us to conclude that all the failures are generated exclusively from the 6T SRAM cell. There has already been reports on 6T SRAM reliability analysis which were relying only on the supply voltage [45] or temperature [46] variations. This is the first reported integral reliability study which takes into account both the supply voltage and temperature variations. The automated simulation environment is presented in Fig. 3.4.

Following the simulation procedure described earlier, we have performed Monte-Carlo simulations under variation of MOS transistor parameters, temperatures and supply voltages. We identified three different regions depending on the supply voltage that is applied to the 6T SRAM cell. The detailed explanation for each operation region is provided below, taking into account how both the supply voltage and the temperature affect the reliability of 6T SRAM cell.

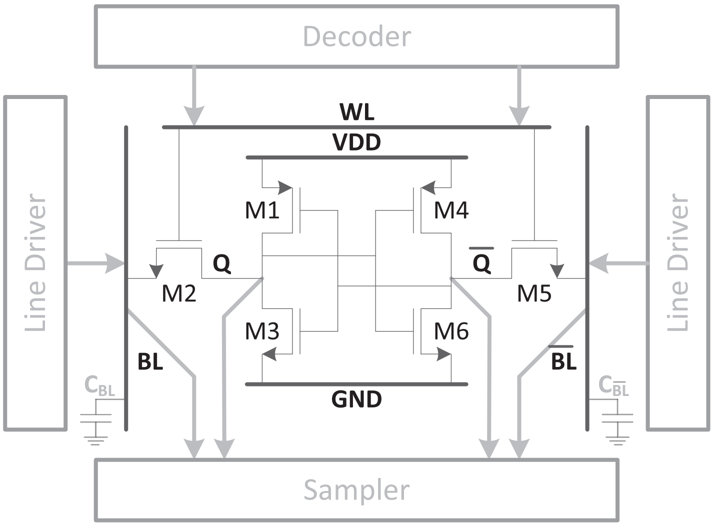


Figure 3.4: Automated VerilogA Based Simulation Environment.

For the supply voltages in between nominal 1.8 V and 1.1 V, we did not register any failures at all the temperatures up to 125°C. This result is strongly in line to our predictions that, due to its positive feedback loop coupled inverters, the standard 6T SRAM cell is inherently robust to the operation under elevated temperatures. The FR (*Failure Rates*) results versus supply voltage variations at high temperatures are presented in Fig. 3.5.

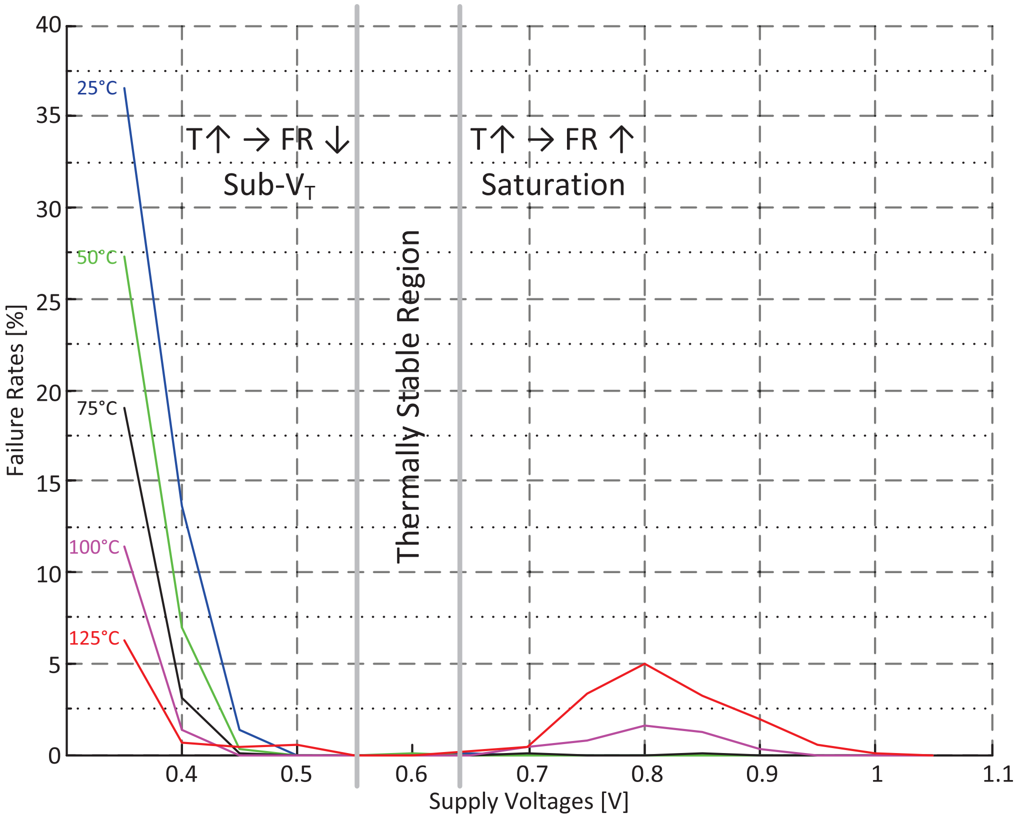


Figure 3.5: The Failure Rates vs Supply Voltage Variations at High Temperatures.

The three dominant regions characterized by the same FR trends are identified as following:

• Saturation region: Assuming supply voltages decreasing from 1.1 V to 0.7 V, we see the trend of increasing the FR as the supply voltage drops. This trend is particularly obvious in between 1.0 V and 0.8 V. In the saturation region, elevated temperature increases FR at every given supply voltage. At 0.8 V, the FR = 2 % at 100°C increase to the FR = 5 % at 125°C, as presented in Fig. 3.6.

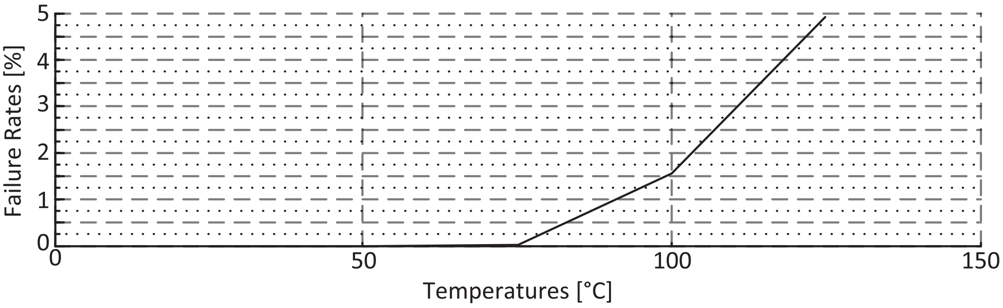


Figure 3.6: The Saturation Region Failure Rates at High Temperatures.

• Thermally stable region: when applying supply voltages in between 0.55 V and 0.65 V, the 6T SRAM cell is thermally stable and does not fail over the whole temperature range. The reason for that could be found in the fact that both the drain current and gate capacitance of the transistors which are found in inverters inside the 6T SRAM cell are thermally independent in this operation region. It turns out that this region is equally reliable comparing to the operation under nominal supply voltage of 1.8 V and room temperature of 25°C.

• Sub-threshold region: Assuming supply voltages decreasing from 0.5 V to 0.3 V, we see the trend of increasing the FR as the supply voltage drops. In the sub-threshold region, elevated temperature decreases FR at any given supply voltage. Such trend is completely opposite to the trend we observed in the saturation region. At 0.4 V, the FR = 15 % at 25°C decrease to the FR = 9 % at 50°C, as presented in Fig. 3.7.

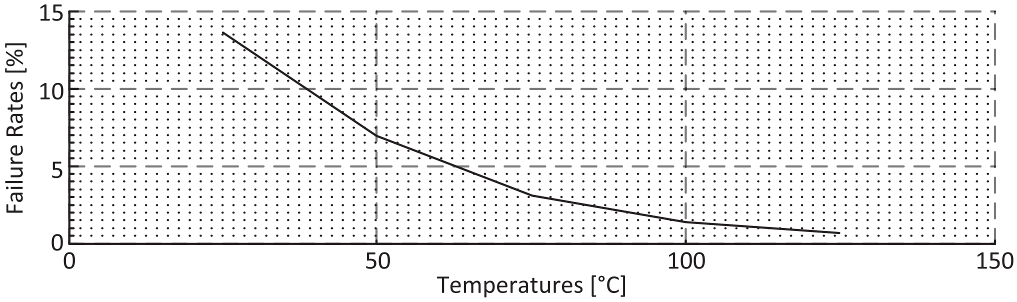


Figure 3.7: The Sub-threshold Region Failure Rates at High Temperatures.

3.3.2 Analysis of the 6T SRAM Cell Failure Rates Results

The FR are divided into four failure types we defined earlier. As we can see in Fig. 3.8, the Write failures (W0 and W1) are dominating the Read failures (R0 and R1) and the trend is similar for both the super-threshold and sub-threshold regions. Also, it is important to mention that the readout is almost ideal one and that in silicon implementations FR are increased due to the voltage differences in between the BL and $\overline{BL}$ which are needed for the proper operation of sense amplifiers. This differential voltage is usually in order of 10 mV to 100 mV.

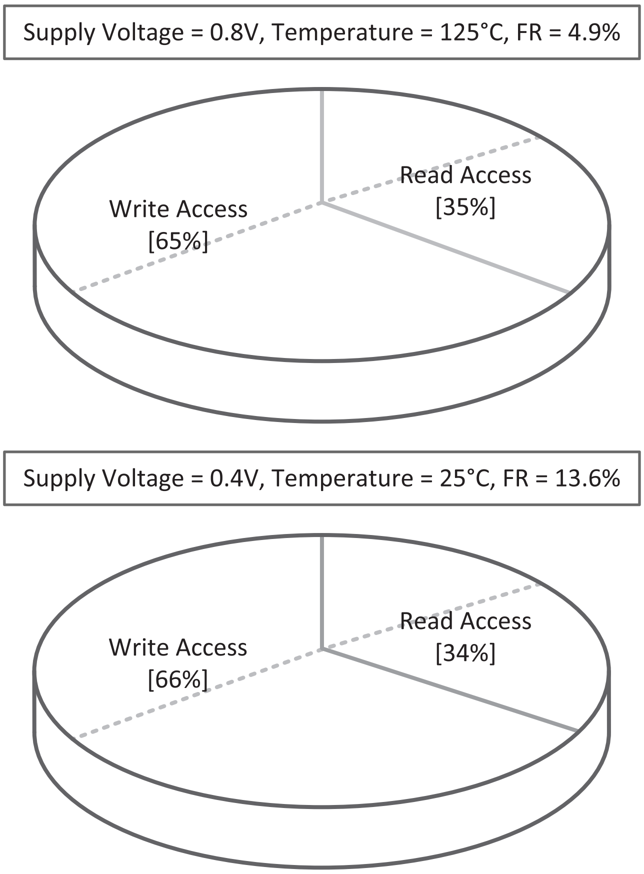


Figure 3.8: The Failure Types Ratios in Saturation and Sub-threshold Regions.

The thermally stable region is the object of our particular interest, because it brings back reliability to the 6T SRAM cell operation. This operating point is very well known as the *Near-threshold voltage operation*. It has already been used for the 8T SRAM design in [44]. In order to explain this phenomenon, first we must analyze MOS transistor parameters at elevated temperatures.

Essentially, the 6T SRAM cell uses current to change its state (Write access) or to drive the BL and $\overline{BL}$ (Read access). That is why we simulated the MOS transistor drain currents under elevated temperatures. The simulation results are presented in Fig. 3.9.

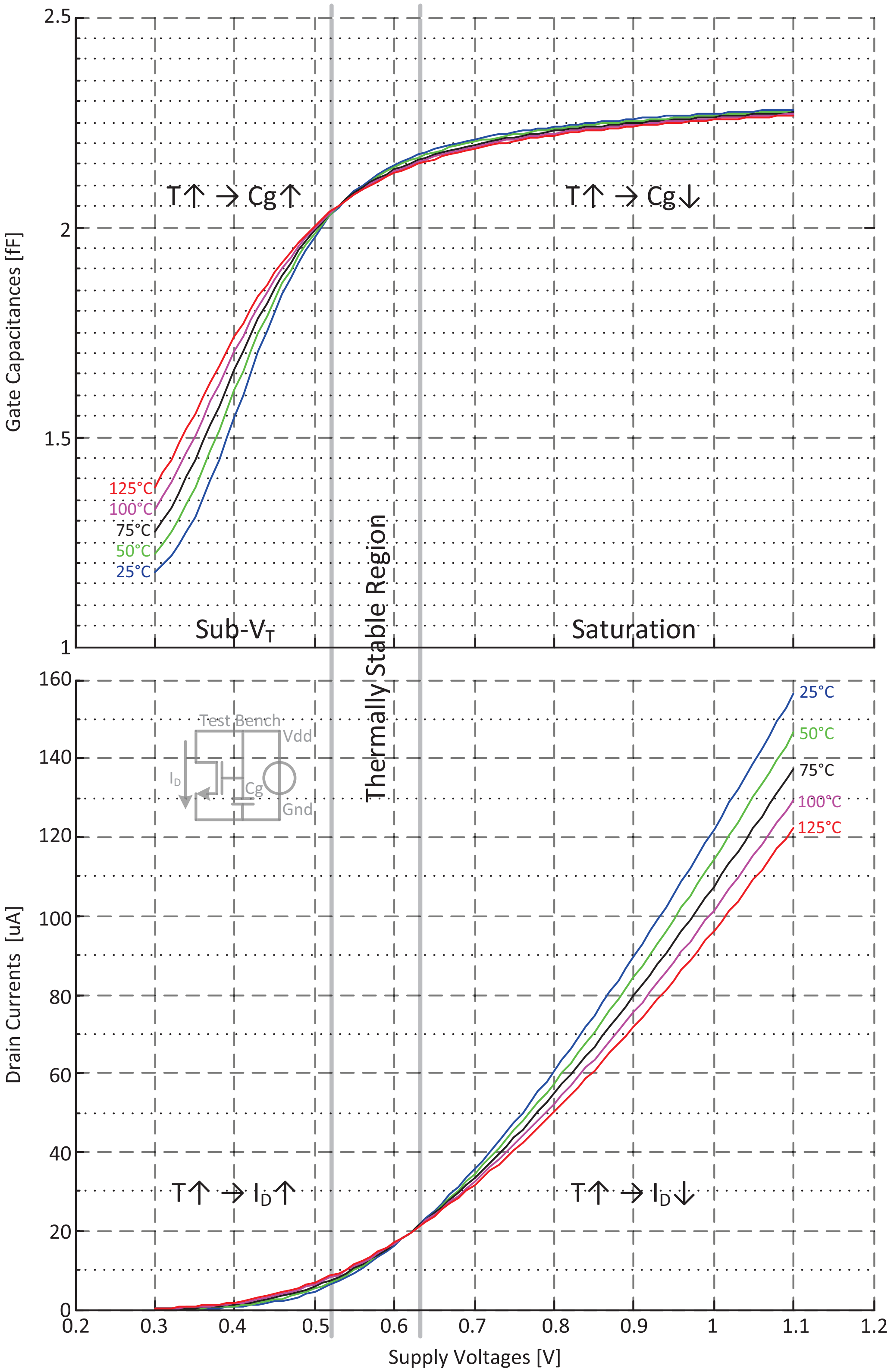


Figure 3.9: Drain Currents and Gate Capacitance at High Temperatures.

As it can be observed, the drain currents are almost constant while the MOS transistor operates in the thermally stable region, where the stronger positive sub-threshold dependence of current versus temperature transitions into a weaker negative super-threshold dependence versus temperature. This simulation result can be directly used to explain why there are no failures during Read accesses. While performing a Read access (R0 and R1), a 6T SRAM cell drives voltage levels of the BL and $\overline{BL}$ by charging/discharging their capacitance. Using previously described ideal capacitors within the simulation environment, it turns out that the constant amount of drain current is sufficient to successfully charge/discharge capacitance each time. This explains nonexistence of the Read access failures in this region.

In order to explain nonexistence of Write accesses (W0 and W1) failures, we must take into account another important MOS transistor parameter. The gate capacitance is charged/discharged by drain current each time the 6T SRAM cell changes the value it holds in the Q and $\overline{Q}$ nodes. That is why we simulated the MOS transistor gate capacitance under elevated temperatures. The simulation results are presented in Fig. 3.9.

As it can be observed, the gate capacitance have almost constant values while MOS transistor operates in the thermally stable region. Taking into account that drain currents have equally constant values in this region, we can make the same conclusion as for the Read access failures. Thus, the constant amount of drain current is sufficient to successfully charge/discharge thermally constant capacitance each time. This explains nonexistence of the Write access failures in this region.

Nevertheless, since this thermally stable region is relatively narrow in terms of operating voltages and dependent on the threshold voltage variations, it may not be used as a very reliable mean to achieve temperature-independent operation.

3.3.3 Reliability Improvements of the 6T SRAM Modules

As we already proved by simulation results, the 6T SRAM cell is inherently robust to supply voltage and temperature variations. Further reliability improvements would assume modifications outside the 6T SRAM cell, mainly in the peripheral circuitry. This research field lacks reliability reports on sense amplifiers operation at high temperatures.

We have seen that the 6T SRAM pass transistors (M2 and M5) do not have body contact which prevents current conduction in both directions. Such floating-body SOI MOS transistors are very much sensitive to temperature variations and they suffer from threshold voltage variations and high leakage currents. Driving strength of these transistors is quickly degraded due to thermally-caused drain currents decreasing and leakage currents increasing. The driving strength (I_{ON}/I_{OFF} ratio) temperature dependence is presented in Fig. 3.10.

This performance degradation is not visible on the reliability analysis of the stand-alone 6T SRAM cell, because the built-in cross coupled feedback mechanism largely prevents failures. Its impact to the overall SRAM module operation manifests in the readout and sense amplifiers operation. Once the driving strength of those transistors is decreased, sense amplifiers face serious problems to detect the differential voltage levels. That is why we propose to improve reliability by more digital design. The 6T SRAM cell could be replaced by a single-ended fully-digital D latch. The fully-digital SRAM module completely eliminates pass transistors as well as sense amplifiers and uses exclusively SOI MOS transistors with the body contact.

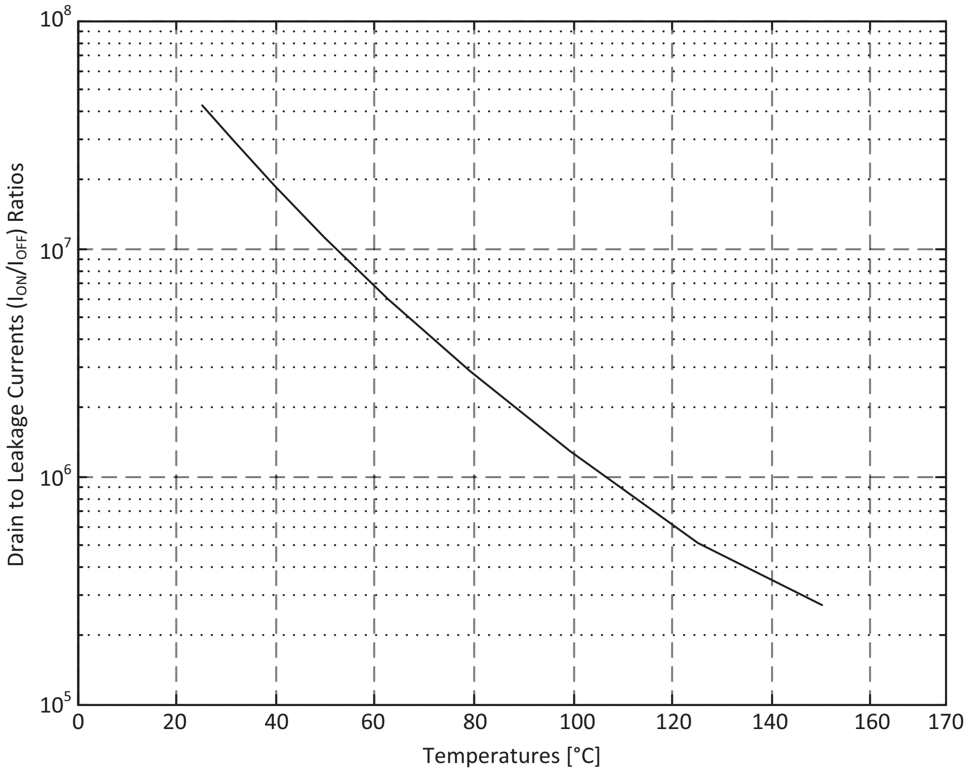


Figure 3.10: Pass Transistor Drain and Leakage Currents at High Temperatures.

3.4 Latch-based SRAM for Operation at High Temperatures

Unlike 6T SRAM modules which need to be recreated for each new technology using dedicated memory compiler, the use of Latch based SRAM modules described in an HDL simplifies the portability of a design to any other technology. In addition, Latch based SRAM can be described in a generic way, where the number of words (Address Size) or the number of bits per word (Memory Word Size) are specified at design time. Once described in the HDL, Latch based SRAM modules can be placed automatically using the same placement tools as for the other standard cells, whereas 6T SRAM modules need to be placed manually. Despite these advantages, the Latch based SRAM module is significantly larger comparing to the 6T SRAM module of the same memory size. The area overhead increases with memory size and is technology dependent [47].

The Latch based SRAM module consists of the following building blocks, known as *Write logic*, *Read logic* and *Array of storage cells* [47]. Typical 1 kB Latch based SRAM module top level architecture is presented in the Fig. 3.11. Memory layout consists of 1024 × 1 words, where one word contains eight bits.

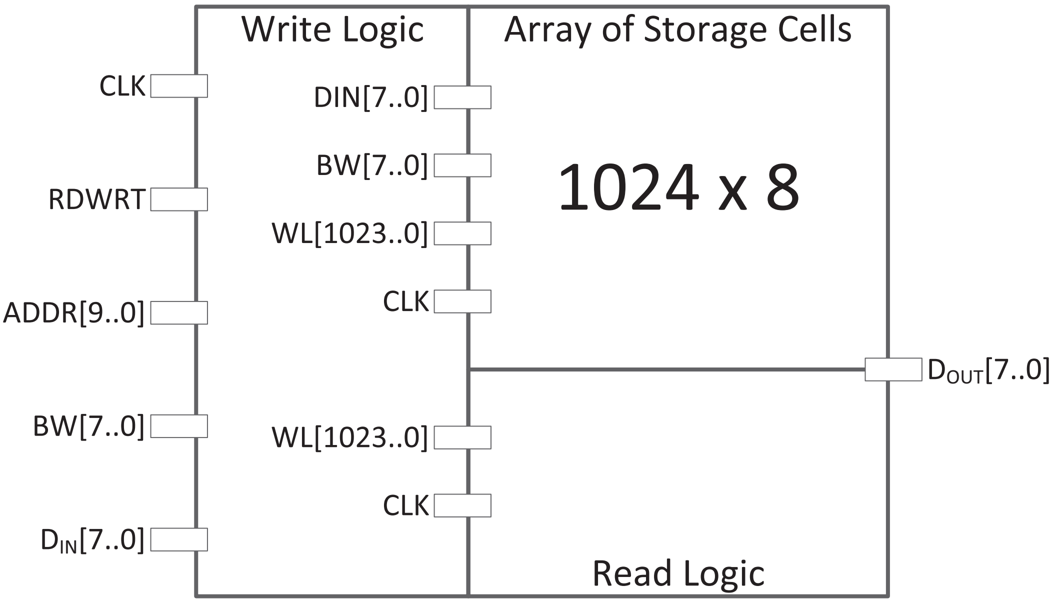


Figure 3.11: The Top Level Architecture of the Latch Based SRAM Module.

3.4.1 Latch based SRAM Cell

In Latch based SRAM modules, an SRAM cell stores data using a simple D latch. All the SRAM cells in one row share the same decoded WL signal and the corresponding bit write control signals, $BW[7..0]$, in conjunction with clock-gating cells. Those three input signals to a Latch based SRAM cell are creating a clock-enable signal, CLK_{EN}, for the internal D latch. The Latch based SRAM cell architecture is presented in Fig. 3.12.

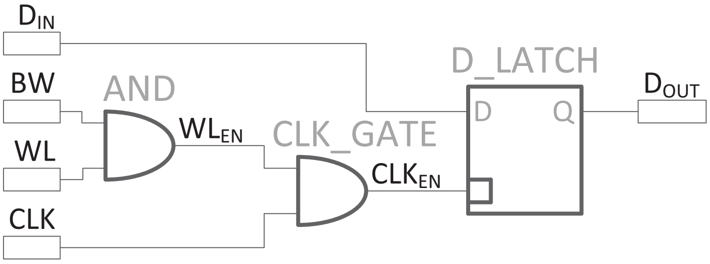


Figure 3.12: The D Latch SRAM Cell.

It consists of three standard cells, where the D latch is used to store a memory bit. The other two gates are used for write access control, where the specific clock-gating standard cell is used to prevent functional hazards which may occur as a result of glitches. Any glitch activity in clock gate enable signal may result in storing undesired value and can jeopardize the correct functioning of the entire SRAM module. The main operation principles of the Latch based SRAM cell are presented in Fig. 3.13.

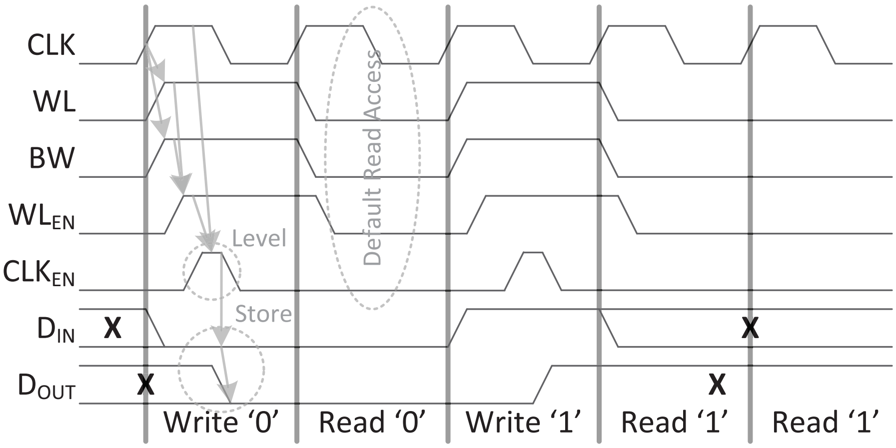


Figure 3.13: Operation Principles of the D Latch SRAM Cell.

3.4.2 Write Logic

The Write logic selects an SRAM cell using the decoded address $WL[1023..0]$ and bit write control signals $BW[7..0]$. The content of the corresponding cell is updated accordingly on the next rising-edge. This is accomplished by the write address decoder that decodes signal $ADDR[9..0]$ into signal $WL[1023..0]$. This signal is One-Hot encoded and selects one row of the storage cells array. Finally, the selected cells need to update their state according to the input data $D_{IN}[7..0]$ to be written. Two Write accesses (W0 and W1) are presented in Fig. 3.13.

It is possible to observe the exact moment when the D latch store its new value. The signal WL_{EN} is formed by conjunction of the WL and BW signals. The WL_{EN} and CLK signals create CLK_{EN} signal in the clock gating cell. This signal is used to enable the D latch that is level sensitive. Once this CLK_{EN} pulse meets the hold time requirements of the D latch, the new value has been stored successfully.

3.4.3 Read Logic

The Read logic is usually a combinatorial network. Typical one clock cycle latency is obtained by inserting simple D flip-flops at the data output signal $D_{OUT}[7..0]$. Routing one word content to the output is done using Write logic's decoded address signal $WL[1023..0]$ that enables the addressed word to provide the content to the output. This value is further passed to the latency register that holds the SRAM data output signal $D_{OUT}[7..0]$, until the next Read access. Two Read accesses (R0 and R1) are presented in Fig. 3.13.

It could be observed that there is not any decoding activity needed for the readout of the Latch based SRAM cell, unlike in the 6T SRAM cell. This leads to the conclusion that this SRAM cell has a default Read access. Such property leads to reduced power consumption at the cell level comparing to the 6T SRAM cell.

3.4.4 Design Summary

The setup and hold times presented in Fig. 3.2 and Table 3.2 are constraining maximum operating frequency, f_{MAX}, particularly the following: T_{as}, T_{ih} and T_{out}. Minimum clock period that met the longest setup and hold times is defined by T_{as} and T_{dh}. It is equivalent to 6.6 ns at room temperature which equals to the operation frequency of 150 MHz. However, simulation showed maximum operating frequency of 50 MHz at 145°C and we decided to design the Latch based SRAM module that operates at that specific frequency at 145°C. Such design decision has been made to enable comparing performance of the two SRAM modules at elevated temperatures. We intentionally sacrificed the Latch based SRAM performance at room temperature.

A preliminary synthesis for various number of rows (from 8 to 16 kB) is performed in order to have a first order estimation of the area dependence of the write address decoder to the number of rows for the Latch based SRAM module. A One-Hot decoder is the best choice in combination with the One-Hot readout multiplexer with respect to the overall Write and Read logic joint area. Address decoding is observed to be the ultimate performance bottleneck of this design. The larger Latch based SRAM modules would suffer from serious performance loss, since address decoding would enlarge the access times significantly [47].

3.4.5 Implementation of the SOI SRAM Modules

The 6T and Latch based SRAM modules are both fabricated on the same die in standard CMOS 0.18 μm SOI process. The SOI SRAM chip layout is presented in Fig. 3.14.

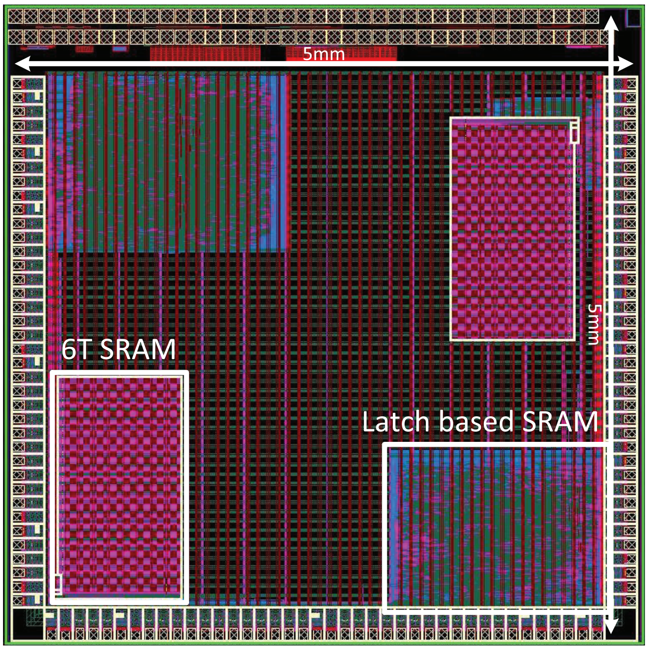


Figure 3.14: The SOI SRAM Chip Layout.

The SOI SRAM chip microphotograph is presented in Fig. 3.15.

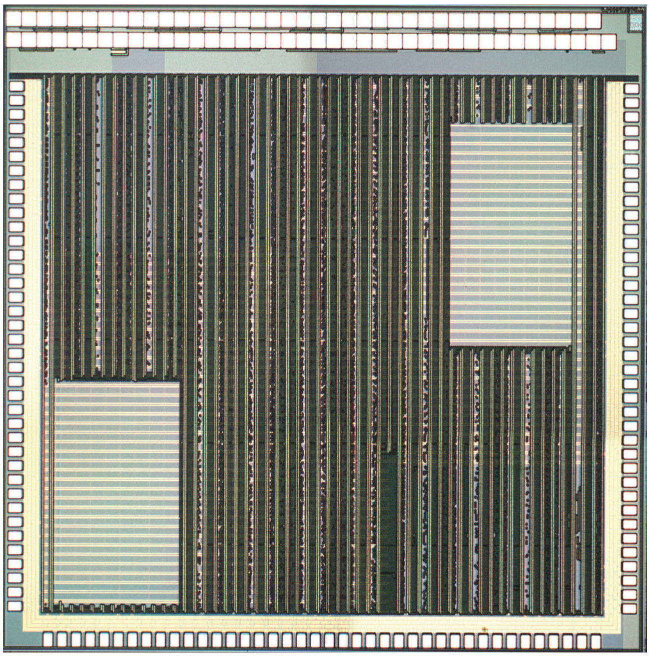


Figure 3.15: The SOI SRAM Chip Micro-photograph.

Latch based SRAM modules are sharing the power rings, VDD and GND, with the rest of the chip, while 6T SRAM modules have their own custom supply. The 6T SRAM module is placed at the lower-left corner and Latch based SRAM module at lower-right corner. The two modules are using all the I/O cells of the bottom chip edge and some on the left and right sides. Two SRAM modules are using separate clock signals and the same I/O and core supply rings.

3.5 Measurement Results

Measurements assume the same set of tests that are used for the verification of the design. It consists of already mentioned repetitive test sequence, W0-R0-R0-W1-R1-R1, executed in the March C order [48]. Every March C test takes 147466 clock cycles, having that for the slowest test takes 147.5 ms while the SRAM module is operating at 1 MHz.

3.5.1 Room Temperature Measurements

The whole concept of the Latch based SRAM replacing its conventional 6T precursor is based on the assumption that the Latch based SRAM modules ars more reliable while operating at high temperatures. That is why we used 6T SRAM room temperature (25°C) performance as the starting point in the comparison of the two memory modules.

We measured its maximum operating frequency, f_{MAX}, and total power consumption, P_{TOT}. These two are the most important performance indicator after the maximum operating temperature. All the memory tests assumed proper March C algorithm execution.

The maximum operational frequency of an on-chip SRAM module is the most important performance indicator. These modules are often used as the on-chip memory that holds compiled instruction code or as the data (tag) cache. Thus, its access time is usually the bottleneck of modern SoCs. We measured the maximum reliable frequency of 42 MHz for the 6T SRAM and 36 MHz for the Latch based SRAM. This is the last point where the March C executes properly without failure and further increasing the operating frequency results in failures.

Stand-by static current is 10 mA for the whole SOI SRAM chip and greater part of it came from the I/O power ring consumption (8 mA). The core consumes as low as 2 mA. Low static leakage current of just 2 mA for stand-by regime is an excellent measurement result for the 50 k gate equivalent design, whit respect to the 2-input CMOS NAND gate. This result strongly verifies our expectation of low-leakage SOI process operation.

3.5.2 High-Temperature Measurements

The 6T SRAM performance degrades significantly beyond 150°C. This point is a threshold for the high temperature effects in this SOI process, mostly because of decreased carrier mobility and increased intrinsic carriers generation. Until reaching this point the maximum operating frequency and total power consumption are close to the room temperature (25°C). Beyond this point, the maximum operating frequency is significantly decreased and the power consumption is strongly increased. Measurement results of the maximum operating frequency and corresponding power consumption are presented in the Fig. 3.16 and 3.17, respectively. The maximum operating temperature is 260°C and the 6T SRAM module is able to perform the March C successfully at 5 MHz.

The Latch based SRAM module has slightly different threshold point for the high temperature effects comparing to the 6T SRAM module. The Latch based SRAM is already changing performances at 125°C. On the other hand, the overall trend changes slower comparing to the 6T SRAM for reasons that are explained above. The power consumption is increased much lower comparing to the room temperature (25°C) operation. The maximum operation frequencies at elevated temperatures are less degraded as well.

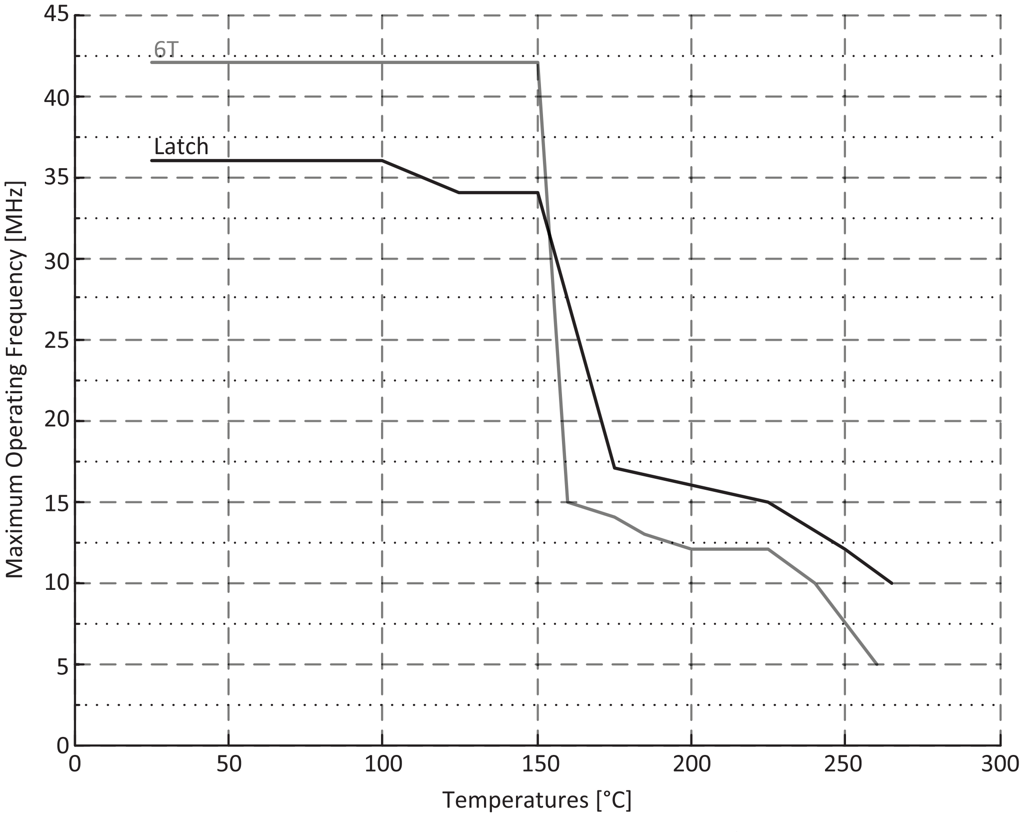


Figure 3.16: Maximum Operating Frequencies at High Temperatures.

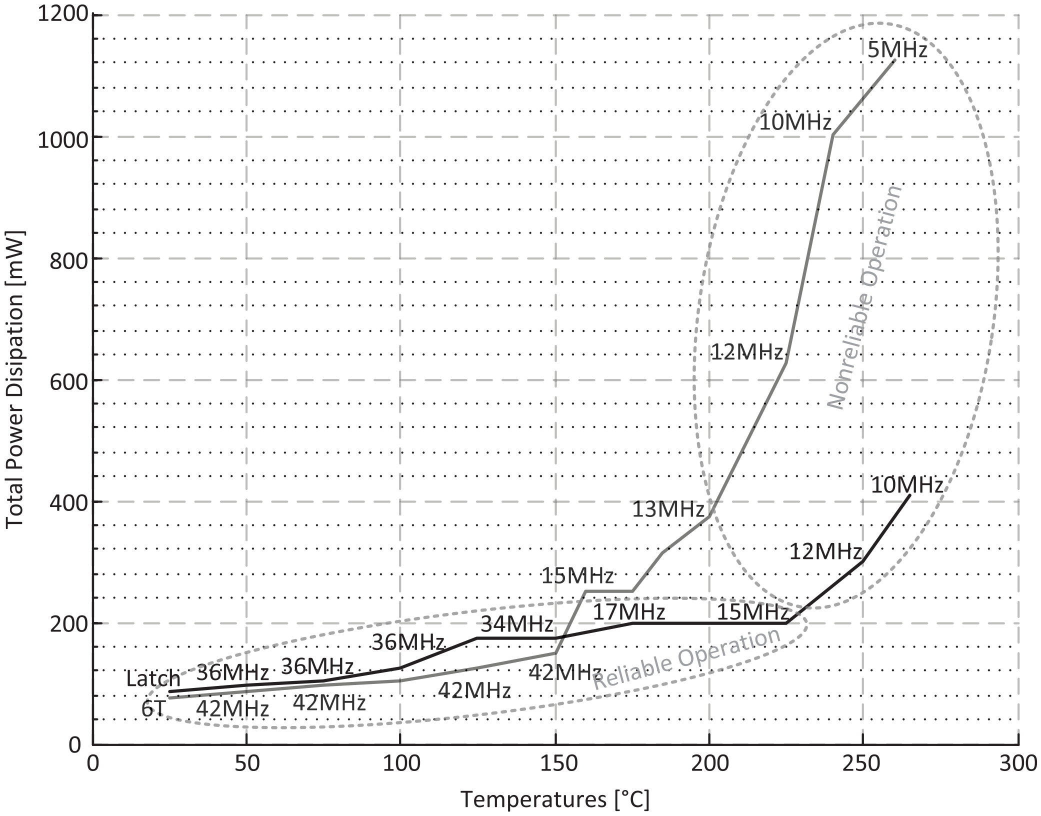


Figure 3.17: Power Consumptions at High Temperatures.

Measurement results of the maximum operating frequencies and corresponding power consumptions are presented in the Fig. 3.16 and 3.17, respectively. Maximum operating temperature is 265°C and the this module is able to perform the March C successfully at 10 MHz. We believe that the Latch based SRAM module is capable of operating at even higher temperatures than 265°C, but it is not possible to measure it using the current test-bench.

Comparison of power consumptions of the two SRAM modules shows clearly that the 6T SRAM consumes much more at elevated temperatures, mainly because of the dramatic drop of I_{ON}/I_{OFF} ratio at high temperatures, especially in floating-body MOS transistors. For example, the 6T SRAM module consumes twice more while operating at 200°C. Going further beyond this temperature, the ratio of the two power consumptions still increases. Thermally-caused increased leakage currents contribute to high ratios which are in favor of the 6T SRAM, mainly by increasing its static power consumption at elevated temperatures. However, the March C test method itself significantly contributes to this ratio. If we recall to the test sequence, W0-R0-R0-W1-R1-R1, we may see that the Write accesses take 33% and the Read accesses take remaining 66%. As explained earlier, when performed over the Latch based SRAM, the Read access does not need any decoding switching activity. That is why the Latch based SRAM consumes less power comparing to the 6T SRAM module. This valuable power consumption measurement result magnifies increased reliability within the Latch based SRAM.

Finally, due to exploding total power consumption, we cannot assume reliable operation of the 6T SRAM at the temperatures higher then 150°C. High power dissipation (over 300 mW) may be destructive for a 50 kGate equivalent design and might cause electromigration failures. In order to reveal these failures, long thermal cycling tests are needed and we were not able to conduct them. On the other hand, the Latch based SRAM module does not consume more then 200 mW until it reaches 225°C. Such total power consumption makes this module more robust for the operation at high temperatures, and comparable in performance to the commercial Honeywell solution [11].

3.5.3 Self-Heating Effect at High Temperatures

The March C test method consists of continuous Read and Write accesses which are known as high power consumption switching activities which motivated us to measure the self-heating effect. We observed that both 6T and Latch based SRAM modules are increasing the die temperature by 25°C while operating at the room temperature of 25°C. This effect is reduced at higher temperatures. For an example, the die heats itself by approximately 5°C at the 250°C. Self-heating effect values are presented if Fig. 3.18. The reason for decreased self-heating value at high temperatures is reduced drain current and reduced operating frequency.

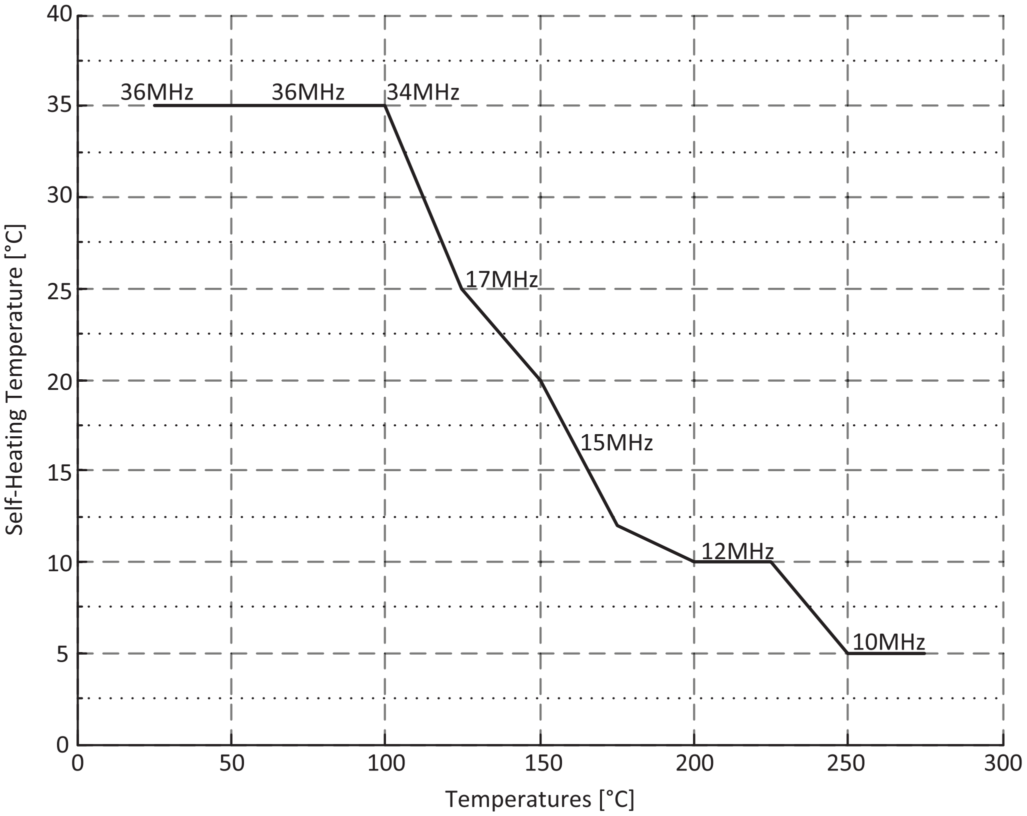


Figure 3.18: Absolute Self-Heating Values at High Temperatures.

3.6 Conclusion

We presented a detailed failure analysis of the 6T SRAM cell. It is the first reported integral reliability study which takes into account both the supply voltage and temperature variations. We proved that the 6T SRAM cell is inherently robust to thermally-caused failures. We determined the nature of these failures and classified them based on the memory access types.

Also, we presented a $0.18\mu m$ SOI CMOS Latch based SRAM for operation at high temperatures. We proved by high temperature measurements that the Latch based SRAM is more reliable compared to the 6T SRAM module. We conclude that it should be used as its substitute when the environment temperature becomes critical (over 150°C). The price to be paid is area overhead for the same memory size SRAM modules and slightly lower operating frequency at low temperatures. The Latch based SRAM consumes 2.5x less power and is able to operate 2x faster compared to the 6T SRAM at temperatures higher than 150°C. We demonstrate reliable SRAM operation at 275°C ($f_{MAX} = 10\ MHz$, $P_{TOT} = 400\ mW$), that is by far the highest reported operating temperature for digital on-chip SRAM module.

To conclude, the new generation SoCs designed for operation at high temperatures, must have reliable on-chip fully-digital Latch based SRAM modules to maintain proper operation when environmental temperature exceeds 150°C.

4 A PowerPC e200 Based SoC for Operation at High Temperatures

This chapter is dedicated to the Firebird, a PowerPC e200 based SoC for operation at high temperatures. We firstly explain what motivated us to design the world's first PowerPC based SoC that is targeting operation in harsh environment. After that, we present the system architecture, design decisions and implementation trade-offs. Finally, we discuss measurement results and conclude this chapter.

4.1 Introduction

There is a growing demand for SoCs integrating one or more microprocessors, on-chip memories, and a variety of sensors and actuators on a single chip that is capable to operate at high temperatures [40]. For example, automotive applications such as ECU (*Engine Control Unit*) require SoCs that reliably operate in high-temperature environments [49]. Modern aircraft industry also demands microcontrollers and electric motors to operate at high temperatures in order to replace hydraulics. Fully integrated solutions allow better reliability than presently used hydraulic structures which exploit many interconnects, plugs and complex mounting procedures [41]. Downhole oil and gas drilling is the oldest and largest application domain of high-temperature electronics ($T > 150°C$). In this application, the operating temperature is a function of the underground depth of the well (the typical geothermal gradient is $25°C/km$). Advances in technology have motivated the industry to drill deeper, thus there is a constant urgent demand for high-temperature microelectronic devices, particularly microcontrollers that are used for control applications.

In 1991, the PowerPC alliance (IBM Corporation, Motorola Inc., and Apple Computer Corporation) defined the Power (*Performance Optimization With Enhanced RISC*) Architecture [50] [51]. A PowerPC is a general-purpose processor based on a superscalar design [51]. The Power Architecture supports a family of processors that spans a wide range of system and application needs. It also provides a stable base for software, allowing applications that run on one PowerPC core to run consistently on any other PowerPC core. Operating systems can be moved from one processor implementation to another by making minor changes [51] [52].

Already in 1994, PowerPC was used in aerospace communication systems as presented in [52]. In 2001, Honeywell presented a radiation hardened PowerPC e603 based single board computer for avionics applications that operates up to 80°C [53]. The PowerPC e200 based MCP5554 microcontroller by Freescale is often used for real-time control applications and it operates up to 125°C.

As commercially available PowerPC based SoCs are not operational at temperatures above 125°C, the main motivation for this work was to design the first PowerPC based SoC that operates reliably beyond 200°C. To the best of our knowledge, there are not even any previous reports on experimental PowerPC processors operating beyond 125°C. Nevertheless, Table 4.1 compares the features and performance of the best commercial PowerPC based SoCs (reaching the highest temperature so far) with this work. Maximum operating temperature, Tj_{MAX}, frequency, f_{MAX}, and total power consumption, P_{TOT}, are taken from product datasheets.

Table 4.1: PowerPC Based SoCs for Operation at High Temperatures.

Manufacturer	Freescale	e2v Semiconductors	EPFL
Model	MPC5554	PC7447A	Firebird
PowerPC core	e200	Dhrystone	e200
Tj_{MAX} [°C]	125	125	225
f_{MAX} $[MHz]$	132	166	38
P_{TOT} $[W]$	-	18	1.45
Cache Size $[kB]$	32	64	32
SRAM Size $[kB]$	64	-	64

4.2 Top Level Architecture

Core e200 is a single-issue (where one instruction is being issued per clock cycle) 32bit Book E Power Architecture [54] compliant core. Its seven pipeline stages with in-order execution feature a 64bit GPR (*General-Purpose Register*) file, a BPU (*Branch Processing Unit*), an LSU (*Load/Store Unit*) and an MMU (*Memory Management Unit*) with 32-entry fully associative TLB (*Translation Look-aside Buffer*) and multiple page-sizes support. The core e200 uses 32kB of 8-way set-associative unified cache. Accelerated processing is supported for integer and single-precision floating-point operations using 64bit operands. Most of the instructions are executed in a single clock cycle, while integer and floating point multiply and multiply-accumulate take three clock cycles and these multipliers are fully pipelined. The top level architecture of the PowerPC e200 core is presented in Fig. 4.1.

The core e200 addresses memories and peripherals using the ARM Ltd. AMBA (*Advanced Microcontroller Bus Architecture*) and it is the only AMBA master in the system. The AMBA consists of the AHB (*Advanced High-performance Bus*) and APB (*Advanced Peripheral Bus*) buses that are connected with a bridge. The AHB addresses directly the RAM and ROM controllers, interrupt controller, parallel port and the AHB/APB bridge. The AHB/APB bridge is master to the APB and it addresses all the remaining peripherals in the system.

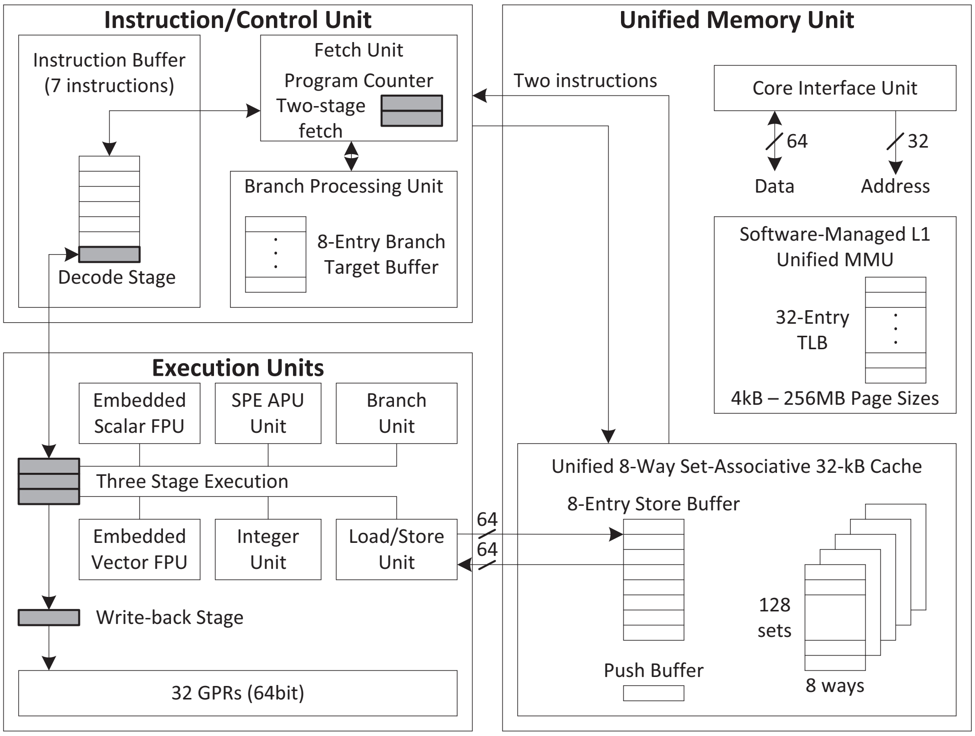


Figure 4.1: The PowerPC e200 Top Level Architecture.

Apart from the PowerPC e200 core and AMBA system, the Firebird SoC has 64kB of both RAM and ROM. The ROM contains compiled boot-up instructions which download the RAM content. The RAM is divided into 32kB instruction and data sectors. The interrupt controller handles eight internal and two external interrupt sources. A reset manager ensures proper system power-up and external reset signal detection. The clock manager allows dynamic frequency reduction while operating at high temperatures. It also provides four external buffered clock sources. Communication interfaces include four SPI masters and two RS232 UARTs. Both interfaces are configurable through internal registers. Finally, a parallel port (programmable interface to external memory) and general-purpose input/output port are available for debugging and application-specific purposes.

4.3 Design Implementation of Firebird SoC

The top level architecture of the Firebird SoC is presented in Fig. 4.2. Firebird SoC design consists of 8 million transistors that are found exclusively in standard-cells and SRAM modules, since it does not infer any analog blocks. It was fabricated in a 0.35 μm CMOS process optimized for low-leakage high-temperature operation. The 142 I/O pins are presented in Fig. 4.2. The remaining pins are dedicated to the power supply.

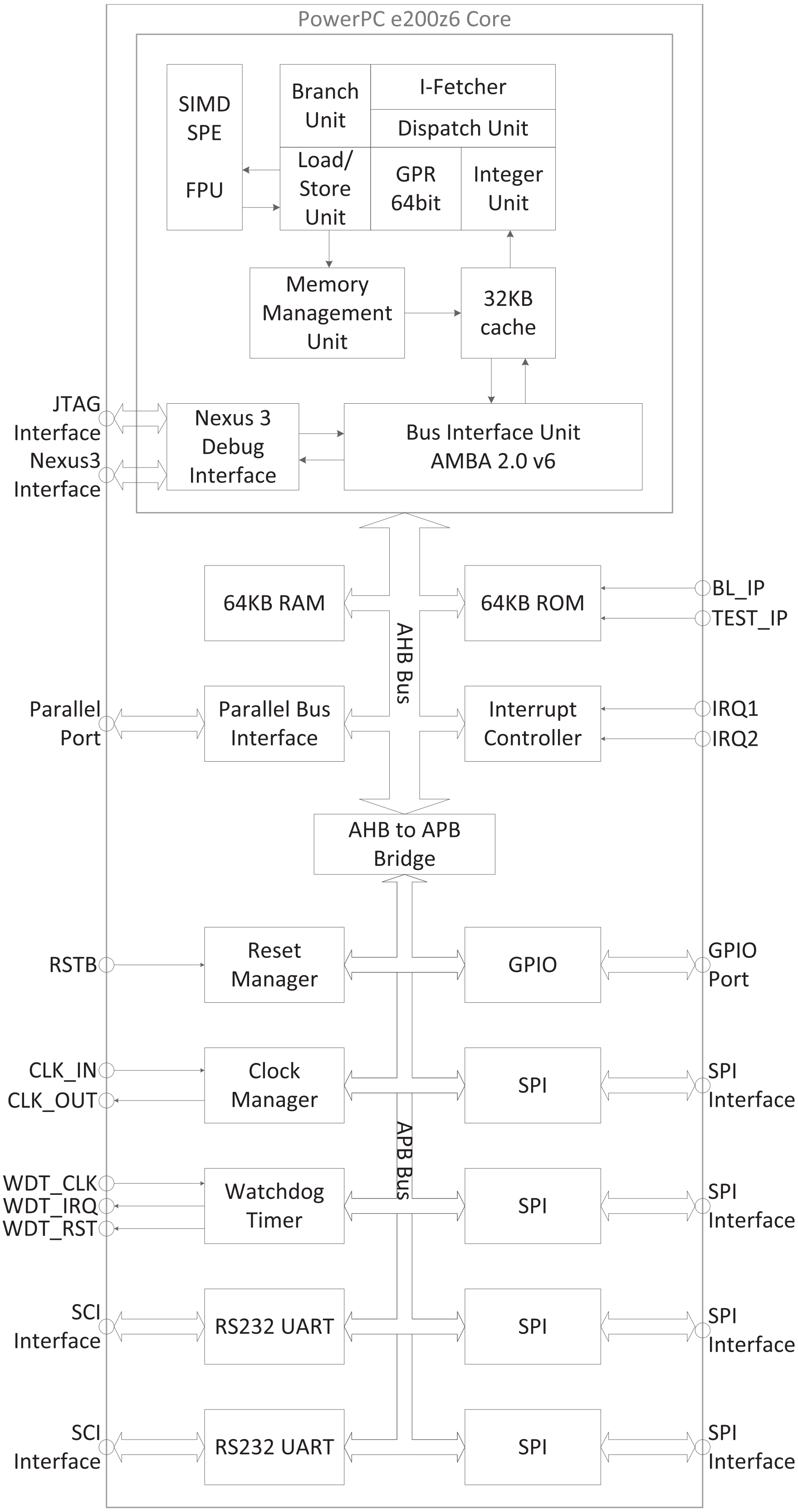


Figure 4.2: The Firebird SoC Top Level Architecture.

The core e200, containing 1.2 million transistors, accounts for the major part of the standard cells, equivalent to 320 kGates, where minimum driving strength two-input NAND CMOS logic gate is taken as reference gate. The 64kB SRAM are implemented in 4x 16 kB SRAM macros and 32kB of Cache memory are implemented in 24x SRAM macros. Overall, those 96 kB SRAM count 4.8 million transistors. The 64 kB on-chip ROM is implemented in a single block containing 2 million transistors.

4.3.1 Design for Operation at High Temperatures

When applied externally, a thermally-stable clock signal with a constant frequency can jeopardize the proper execution of the critical paths, since the maximum operating frequency is degraded due to the reduced carrier mobility at high temperatures [55]. The clock manager supports dynamically reconfigurable frequencies of the clock signal and the capability to internally scale-down the clock frequency. The control of frequency at high temperatures is implemented in software.

Firebird SoC is designed to keep the active power consumption as low as possible over the entire operation range. The goal is to eliminate switching activity in registers when related outputs are not used by fetched instruction or selected operation mode. The switching activity is eliminated when the corresponding clock signal is idle. The clock is exhaustively gated, having as much as 77% of the registers fed by the gated clock. Depending on the operation modes and fetched instructions, all the major PowerPC core parts could be restricted from the clock, including the cache controller, MMU, integer and floating-point units. Hence, independently of the operating temperature, the active power consumption is held as low as possible.

4.3.2 Custom Power Distribution Network for Memory Modules

To prevent high voltage drop on power distribution network, the memory modules must be placed as close as possible to the power ring. The width of the memory power rails (W_{VDD}, W_{GND}) must be wide enough to prevent electromigration effects and signal integrity problems due to a voltage drop on the power rails. The minimum required power rail width that meets the electromigration requirements (W_{EM}) is defined by following equation:

$$W_{EM} = I_{DD,RMS} / Jd_{MAX,Al} \, [\mu m] \tag{4.1}$$

where I_{DD} represents root mean squared value of memory power supply current during clock period time in [mA] and $Jd_{MAX,Al}$ represents maximum current density for Aluminum in [mA / μm]. Based on the process parameters, the optimum power rail width which prevents electromigration effects in the power rails is calculated to be:

$$W_{VDD} = W_{GND} = W_{EM} = 40\,\mu m. \tag{4.2}$$

We designed a triple-rail power distribution network which equally distributes power supply current and is robust to electromigration effects. The power supply current equalization is achieved by wrapping each memory module. Such power rail topology additionally reduces the voltage drop and increases reliability. The custom power distribution network is presented in Fig. 4.3.

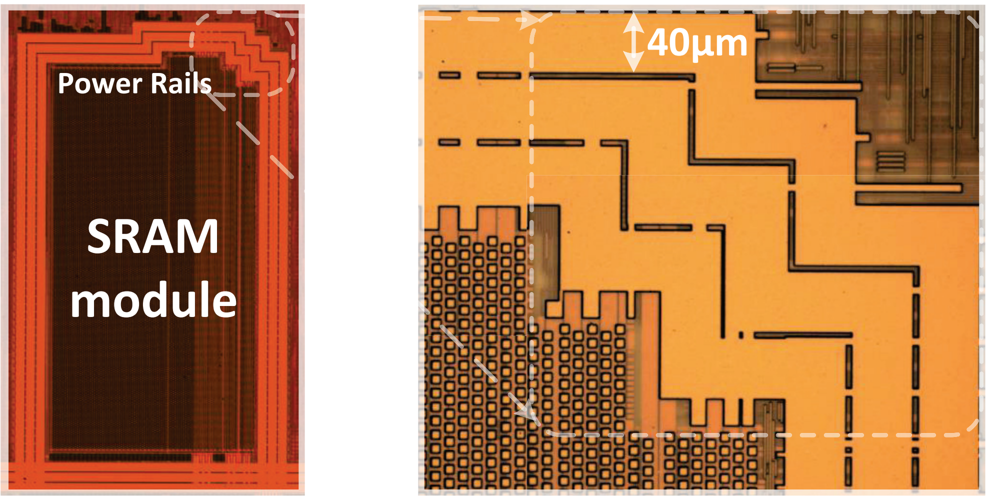


Figure 4.3: The Custom Power Distribution Network.

4.3.3 Reset and Clock Signals Generation

The Firebird SoC operates using several different clocks due to its complex and inherited low-power architecture. That is the reason why very clever and carefully planned clock distribution had to be designed. The Firebird SoC takes the Raw clock signal from the off-chip Quartz Oscillator which is processed by the Clock manager and distributed to the rest of the system.

On the other hand, once the system is powered-up, a proper reset signal is to be applied. This reset signal is also passed to logic that is synthesizing clock which is applied together with the reset for successful start of the operation. It makes no choice than that the Reset Manager provides Power-on-reset using the Raw clock as well. This is the only way to provide meaningful reset and clock signals to the system.

Otherwise, a potentially dangerous loop might be observed in the clock generation:

- Clock Manager gets the Raw clock signal from the off-chip Quartz Oscillator. Then, the Clock Manager bypasses the the system clock to the Reset Manager in order to generate proper Power-on-Reset signal for the whole system including the Clock manager.

- Reset signal is used to reset sequential logic (Frequency Dividers) inside the Clock Manager that is providing system clock signal and the whole system halts by the idle clock. The sequential logic remains silent under the Power-on-Reset signal and there is no system clock that is used to turn-off the Power-on-Reset signal and the whole system remains in the reset state.

That is how the loop in between the Raw and the system clock is created. This potential problem has been anticipated by the Reset and Clock signals generation presented in Fig. 4.4.

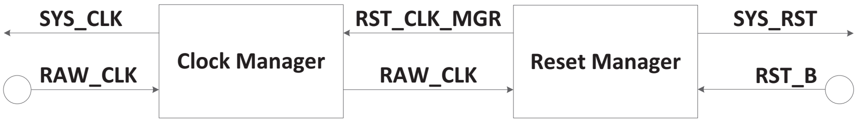


Figure 4.4: The System Reset and Clock Signals Generation.

4.3.4 Clock Gating and Different Clock Domains

Due to its inherited low-power architecture, main computational blocks in the e200 PowerPC are using exhaustive clock-gating. It reduces switching activity in most power-hungry blocks, which results in lower power consumption. From the design aspect, clock-gating is very sensitive routine that must be implemented carefully. If not implemented properly, there will be severe clock behavior resulting in jitter and slack, obtaining malfunction in gated blocks. Gated clocks are presented in Fig. 4.5. Reports show as much as 77% of the registers being gated.

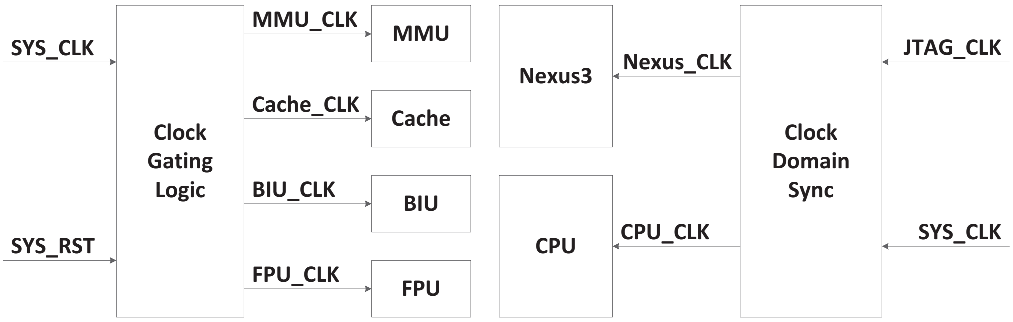


Figure 4.5: Clock Gating and Different Clock Domains.

Besides implemented clock-gating, PowerPC core e200 is running on two different clock domains, one synchronous to the rest of the system and the other one used for debugging purpose – JTAG clock. If not separated properly, two domains may lead to processor's context being lost and generating an exception. Two clock domains are also presented in Fig. 4.5 and the CPU clock is used to run the pipeline, alternating in between the System clock when in normal operation more, and the JTAG clock when in debugging mode.

4.3.5 Interrupts Handling Mechanism

An interrupt is an action in which the processor saves its old context and begins execution at a predetermined interrupt handler address. The Book E Power Architecture defines the mechanisms by which PowerPC core e200 implements interrupts. When an interrupt occurs, information about the CPU state that is held in the MSR and the address at which execution should resume after the interrupt is handled are saved to SRR (*Save/Restore Register*). The core e200 immediately begins executing at the address (interrupt vector) determined by the IVPR (*Interrupt Vector Prefix Register*). Returning from an interrupt is performed by restoring state information from the SRR and PowerPC e200 recommences to fetch instructions from the interrupted flow.

The Watch Dog Timer provides an IRQ (*Interrupt ReQuest*) signal that is directly assigned to the PowerPC e200 and this is defined by the Book E Architecture. The Firebird SoC handles other IRQ signals using an Interrupt controller as presented in Fig. 4.6. The Interrupt Controller multiplexes eight IRQ signals into a single interrupt request that is assigned to the general purpose IRQ port of the PowerPC core e200.

The Firebird SoC contains eight IRQ signals. The SPI and RS232 UART communication interfaces provide four IRQ signals each:

• SPI Interrupt occurs once the SPI communication is completed. Since Firebird SoC implements exclusively SPI Masters, it is the PowerPC e200 core that initiates communication each time and it just needs the confirmation once the communication is done. Therefore, an SPI device implements an interrupt to show that the communication is done, no mater if it is a transmit or receive communication routine.

• RS232 UART device implements two IRQ signals, both for transmit and receive modes, having this device operates in the full-duplex communication mode and those two actions are not necessarily dependent. Once a communication routine is done, a corresponding IRQ signal is asserted.

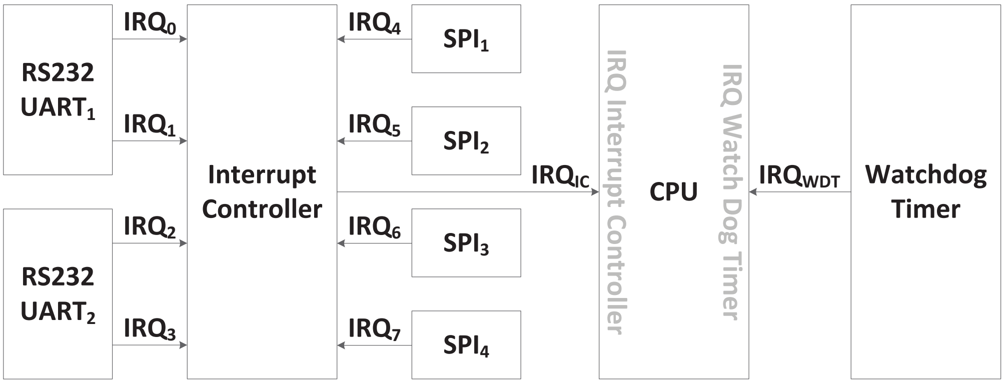


Figure 4.6: Interrupt Handling Mechanism.

4.3.6 Design Summary

The post-place-and-route simulations showed maximum frequency of 33 MHz at 175°C (at 2.75 V supply voltage in the worst case corner). The transistor Spice models are categorized up to this temperature. The critical-path of the Firebird SoC is the on-chip SRAM access which begins at the MMU and ends in the SRAM controller. It starts from the MMU registers and it ends in the SRAM controller.

The process provides only four metal layers including the top metal. Limited metal stack led to reduced standard-cell density (0.6) in order to be able to close the routing of the entire design and resulted in a large die size of 20x9 mm^2. This design uses as much as 256 pins and it is still core limited. The Firebird SoC layout and the chip microphotograph are presented in Fig. 4.7 and Fig. 4.8, respectively.

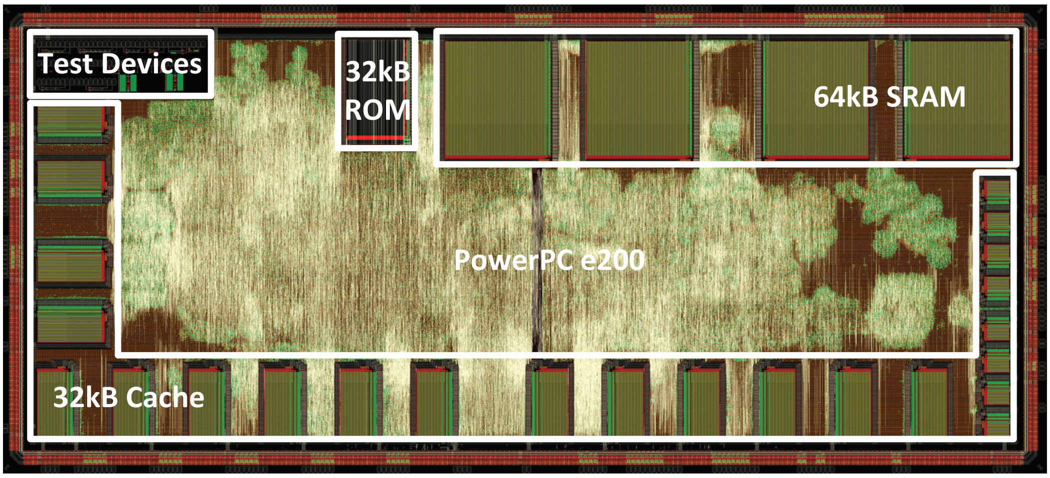


Figure 4.7: The Firebird SoC Layout.

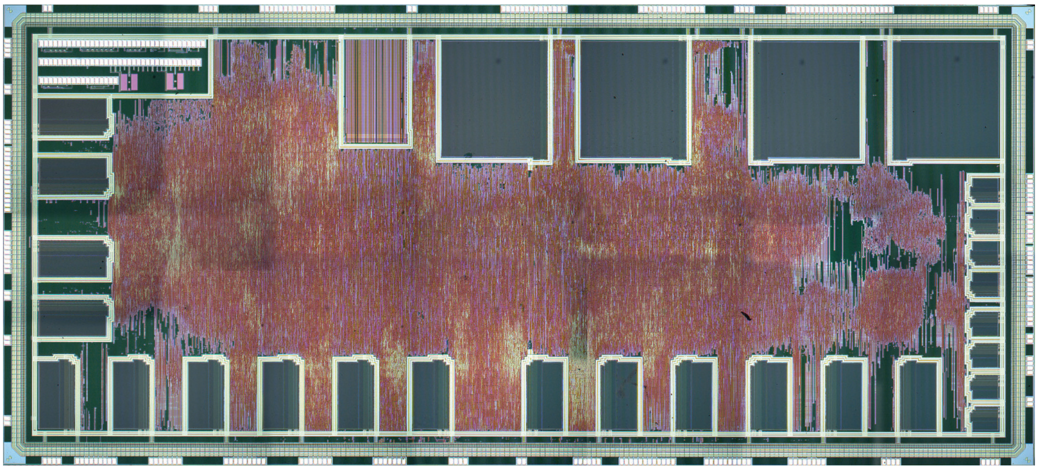


Figure 4.8: The Firebird SoC Microphotograph.

There were multiple design challenges to be solved, but we are going to address and discuss only the most important ones here:

• Cache Distribution: The PowerPC e200 core distributes 32 kB Cache into 24 physically separated modules (16 Data and 8 Tag Cache modules). To illustrate how much of area is occupied, a single 32 kB module is as much as three times smaller. Taking into account the routing to multiple modules interfaces and additional power routing, you end up with four times larger area. There were no possible optimizations or trade-offs possible, since the core architecture (Cache controller) could not be changed.

• Metal Stack: It was almost impossible to route 7 pipeline stages PowerPC e200 core attached to the AMBA bus interfacing SRAM modules – just for the sake of clarification, as of the signal numbers, the AMBA bus infers more than 200 signals. Having Metal1 used inside the standard-cells, Metal3 and Metal4 for the power supply and ground distribution, there is just a single metal (Metal2) that is used for the signal routing. Poor routing capacity led to the decreased density of only 0.6 resulting with serious troubles to close timing constraints. Besides, it enlarged the die area significantly.

The Firebird SoC has been prototyped on an FPGA (Xilinx *Virtex5*) during the development phase. Memory modules were replaced by Block RAMs and the Clock Manager was replaced by the FPGA's DCM (Digital Clock Manager). Besides, there were no differences in between two designs. The FPGA prototype was used for the boot-loader and test code development that was used for the verification and measurements purposes.

To conclude on the design summary, the Firebird SoC is an eight milion transistor design consuming 20 mm x 9 mm silicon die area. It was designed to face critical conditions during the high temperature operation, such as severe behavior of supply voltage, leakage in CMOS logic gates and memories. Post place and route simulations show 33 MHz operation at 175°C.

4.4 Software-Based Self-Test Methodology

When designing a complex SoC for high temperature operation, an efficient verification and testing strategy is needed. Test methodology has to be robust to the high temperature effects and must not fail earlier then the design under test. This leads to the conclusion that commonly used hardware-based built-in self-test (BIST) controllers are not applicable since their failure is completely random with respect to the rest of the system.

Typically, both the BIST and the PowerPC e200 core consist of the same standard-cells and they fail at about the same temperature, so it is impossible to guarantee that the test hardware will survive higher temperatures then the design under test. A software-based self-testing (SBST) running on the PowerPC e200 core is better choice compared to the hardware-based BIST, as it fails at the moment when the PowerPC e200 core is not capable of fetching and executing instructions.

There has already been several successful demonstrations of SBST methods presented in [56], [57] and [58]. However, non of these methods is targeting reliability issues (more precisely, these tests assumed nominal supply voltage and room temperature) that occur when testing an SoC under elevated temperatures. That is why we designed a novel test methodology which encapsulates reliability analysis for operation under elevated temperatures.

Unlike hardware-based BIST, the SBST is not an intrusive method since it applies tests in the normal operational mode of the system [56], while executing dedicated instructions. While executing the test code, PowerPC e200 core disables interrupts and cache memory, making sure that there is no processor context deviation from the test-code execution.

The PowerPC e200 core runs test-code that is stored in ROM. Primary goal is to determine that processor itself is fully operational, having that it will test the rest of the system. This test is usually performed at room temperature, in order to estimate the maximum operating frequency, since the critical path of the system is not inside the processor. Once it is proven that the processor is fully functional, we test the on-chip SRAM.

It has been shown in [43], that the 6T SRAM fails first at the elevated temperatures and that is why the test-code must be stored in ROM and not in the Instruction part of the on-chip SRAM. The Data part of the on-chip SRAM is not used by the test-code to store any variables, having that it might cause the system failure. Instead, these variables are stored in the internal General Purpose Registers (GPR).

When both processor and on-chip SRAM are tested, the test-code checks peripherals, including 2x RS232 UART and 4x SPI. Once the RS232 UART is tested, it is used by the test-code to transmit the test-results. Each test has its own unique code and test-result confirms if the test passed. In case of failure, test-result encapsulates a failure cause.

4.4.1 PowerPC SBST Methodology

The PowerPC e200 core runs two sets of tests. The first portion of test-code is used to determine proper room temperature operation at nominal operating frequency of 40 MHz. This test validates that chip fabrication and bonding were done correctly. The second portion of the test-code is used to perform the tests at elevated temperatures. These tests assumed proper instruction execution which are handled by these parts of the PowerPC e200 core that are the most critical with respect to the high temperature operation. High temperature effects usually cause increased delays in the digital CMOS circuits that lead to improper instruction execution. That is why we tested the critical path of the PowerPC e200 core which differs from the critical path of the whole system.

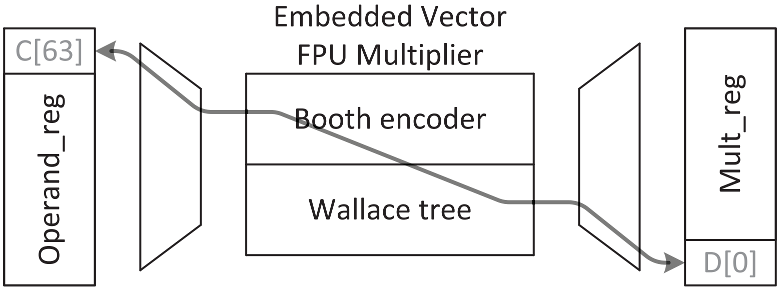


Figure 4.9: The Critical Path of the PowerPC e200.

The critical path of the PowerPC e200 core is located in the FPU multiplier. The FPU multiplier consists of the Booth decoder and the Wallace tree addition of the partial products [59]. This topology is proven to be faster then the Synopsis DW (*Design Ware*) substitute. The FPU multiplier and the critical path are presented in Fig. 4.9.

In order to exhibit the critical path of the FPU multiplier, we implemented SBST algorithm which calculates word-size (32 bit) products in to different ways. The basic idea is to compare the result of the FPU multiplication with the corresponding product that has been generated using the *Shift-and-Add* method. The FPU multiplier SBST algorithm is presented in Fig. 4.10. The FPU multiplier SBST algorithm is executed in the following steps:

• Initially, we load algorithm variables into the $Operand_A$ and $Operand_B$ registers. These values will be used by both the FPU multiplier and the ALU adder. The $Operand_A$ register contains and updates a counter, cnt, that counts in the $[1..maxInt]$ range. The $Operand_B$ register contains a constant, $maxInt$, maximum unsigned 32 bit integer value.

• After the initialization, the FPU multiplier multiplies $cnt * maxInt$ in each iteration and store its value to the $mult$ register. In parallel to that, the ALU adder adds $sum + maxInt$, where the sum represents registered value of previously calculated sum. Thus, output register of both the FPU multiplier and ALU adder contain the same values. This approach guarantees that the APU addition will be always executed faster than the FPU multiplication. The SBST algorithm can catch a failure in the FPU multiplier when clock period is shorter then the critical path delay.

- Finally, the ALU comparator compares $sum <> mult$ resister values. In case that this comparison generates the flag which marks nonidentical values, a multiplication failure is captured. It is always the case that the FPU multiplier fails first, because it has significantly longer propagation delay comparing to the ALU adder (there are 32x 32 bit adders in the Wallace tree of the FPU multiplier).

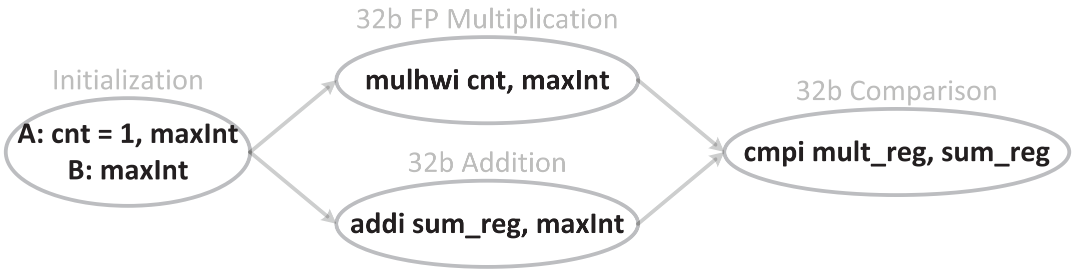


Figure 4.10: The FPU Multiplier SBST Algorithm.

However, we managed to execute only the first set of tests which operates at the room temperature. The second portion of code that was targeting tests under elevated temperatures requested a PowerPC e200 debugger that is capable of stopping the pipeline and forcing it to execute desired instructions, described by the algorithm. It is not possible to execute this portion of code in the traditional way by fetching it from the Instruction section of the on-chip SRAM. Also, this code cannot be executed from the on-chip ROM having that it uses several variables which must be stored in the Data section of the on-chip SRAM.

Later SBST of the on-chip SRAM indicate that this component fails first in the system. The prove for that could be supported by the fact that the SBST is executed from on-chip ROM and using the PowerPC e200 to perform Read and Write accesses. This leads to the conclusion that, at the system level, the PowerPC e200 core is more reliable then the on-chip SRAM. However, it is not possible to determine which part of the PowerPC e200 fails first while operating at elevated temperatures.

4.4.2 On-chip SRAM SBST Methodology

Tests assumed proper March C algorithm [48] execution on the entire addresses range of the 64kB SRAM, consisting of both 32kB Instruction and Data addressable spaces. A March-based test algorithm is a finite sequence of March elements. A March element is finite sequence of operations specified by an address order and a number of reads and writes. An operation can consist of: write-0 (w0), write-1 (w1), read-0 (r0) and read-1 (r1). It has been observed that March C algorithm provides the highest fault coverage with a reasonably low software complexity (making exclusively read and write accesses to the on-chip SRAM). The order of memory addresses is given as ↑, ↓, and ↕ for ascending, descending and irrelevant order. The March C algorithm we used has the March elements structured as following:

$$\updownarrow(w0)\downarrow(r0,w1)\downarrow(r1,w0)\uparrow(r0,w1)\uparrow(r1,w0)\updownarrow(r0) \tag{4.3}$$

This sequence of simplest read and write accesses allows us to test the entire addressable space of the on-chip SRAM. As soon as the data which has been read from SRAM does not match the test pattern (data size is one byte in our case), we declare an SRAM operation failure and send a test message. Test message consists of the address and the pattern that is read with a fault. The test is initially performed at the room-temperature and on-chip SRAM is fully functional, as it was expected. High temperature tests show random failures and it is analysis was very difficult, having that it causes the whole system to fail.

4.4.3 Peripherals SBST Methodology

Two RS232 UARTs were tested by sending hard-coded string from the ROM. Four SPI masters were tested by communicating in loop-back configuration. The reset manger was not tested during the BIST operation, since it had a single functionality (reset generation) that was anyway executed before entering the test-mode. The interrupt controller was disabled during the test-mode, but it was used immediately after, during the boot-up RS232 code download that initialized SRAM. Also, there were no particular tests for the GPIO, but this port was used by all the other tests to send out test results.

4.5 Measurement Results

While executing the SBST at the nominal power supply 3.3 V , the Firebird SoC is capable of operating at $f_{MAX} = 38\ MHz$, while consuming $I_{DD} = 430\ mA$. Room temperature tests were done on three setups and all show similar results.

4.5.1 High-Temperature Measurements Results

The main goal of high-temperature measurements is to determine the maximum operating frequency and related total power (active and leakage) consumption which are the most important performance indicators. The high-temperature measurement results are presented in Fig. 4.11 and Fig. 4.12, respectively.

The maximum operating frequency measurement results strongly verify our prediction that the maximum operating frequency degrades with elevated temperatures. As the post-place-and-route simulation reported 33 MHz at 175°C in the worst case corner, higher maximum operating frequency at room-temperature was expected and the result of 38 MHz is in line with our prediction. Further, we measured the maximum operating frequency of 31 MHz at 175°C that is very close to simulated 33 MHz for the same temperature. This result strongly confirms that technology provided transistor Spice models were accurately categorized under elevated temperatures.

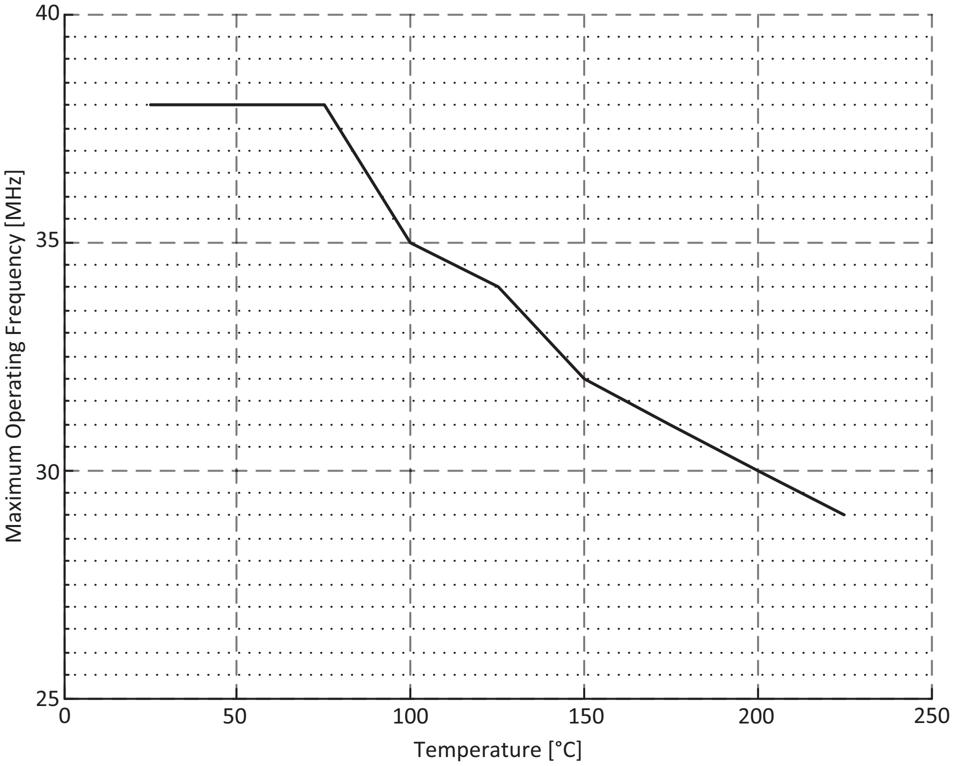


Figure 4.11: The Maximum Operating Frequencies at High Temperatures.

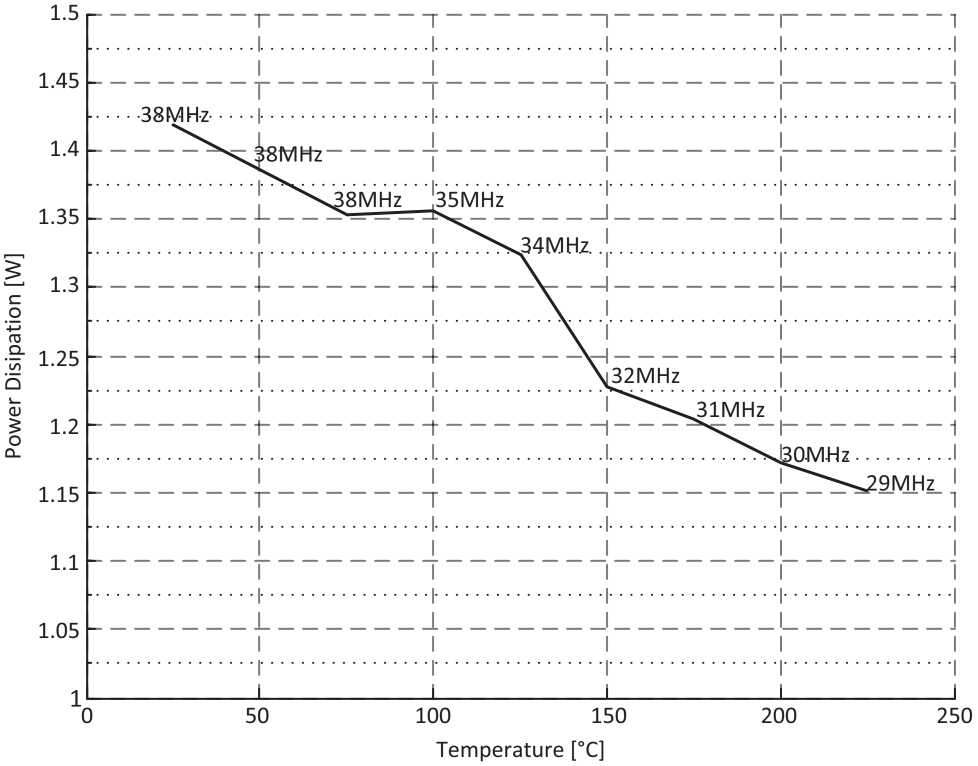


Figure 4.12: The Total Power Consumptions at High Temperatures.

The Firebird SoC performance degrades significantly beyond 75°C. This point is a threshold for the high temperature effects in this Bulk CMOS process, mostly because of decreased carrier mobility and increased intrinsic carriers generation. Until reaching this point, the maximum operating frequency and associated total power consumption are close to the room temperature of 25°C. Beyond this point, the maximum operating frequency is linearly decreased. Maximum operating frequency degradation trend follows the reduction of carrier mobility with respect to temperature [55]. The power dissipation measurements assume the total power dissipation while running at the maximum operating frequency for that given temperature.

The static leakage current increases exponentially with increased temperature. Thus static power dissipation, that is negligible at room-temperature, becomes a significant part of the total power consumption at high temperatures, so the total power dissipation of 1.42 W can be referred to as the highest active power consumption of the Firebird SoC. On the other hand, as the maximum operating frequency is degraded with increased temperature, and the active power consumption is reduced. The peak of the power consumption is when the die temperatures are in between room-temperature and 125°C. The static power increases slower than the active power consumption decreases, thus the measurement results indicate lower total power consumption with elevated temperature. Such behavior increases reliability and proves electromigration-resistant design, considering that the power supply current has the maximum value at the room temperature of 25°C.

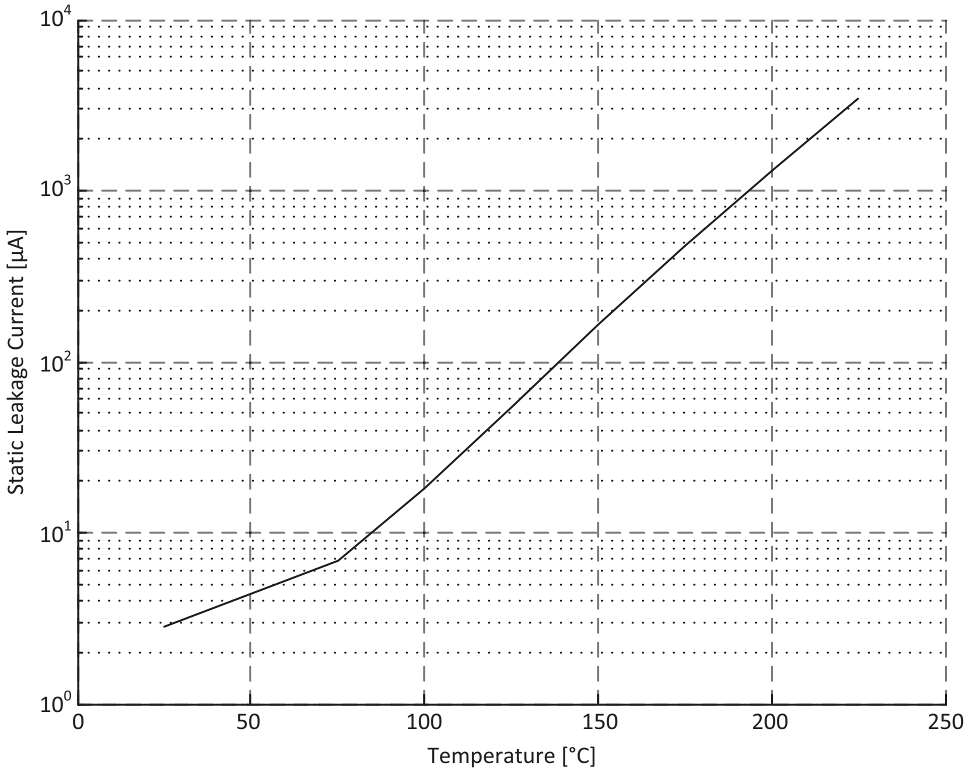


Figure 4.13: The Leakage Currents at High Temperatures.

The leakage currents measurement results at elevated temperatures are presented in Fig. 4.13. When measuring leakage currents, the Firebird SoC was in the idle state which comes right after the Power-on-reset.

4.5.2 Self-Heating Effect at High Temperatures

The SBST method and particularly its essential part, the March C test algorithm, consist of continuous Read and Write accesses. These are known as high power consumption switching activities and they motivated us to measure the self-heating effect. We observed that SBST increases the die temperature by 15°C while operating at the room temperature (25°C). This effect is reduced at higher temperatures. For an example, the die heats itself by approximately 2°C at the 225°C. The reasons for decreased self-heating effect value at high temperatures are reduced drain current and maximum operating frequency. Self-heating effect values are presented if Fig. 4.14.

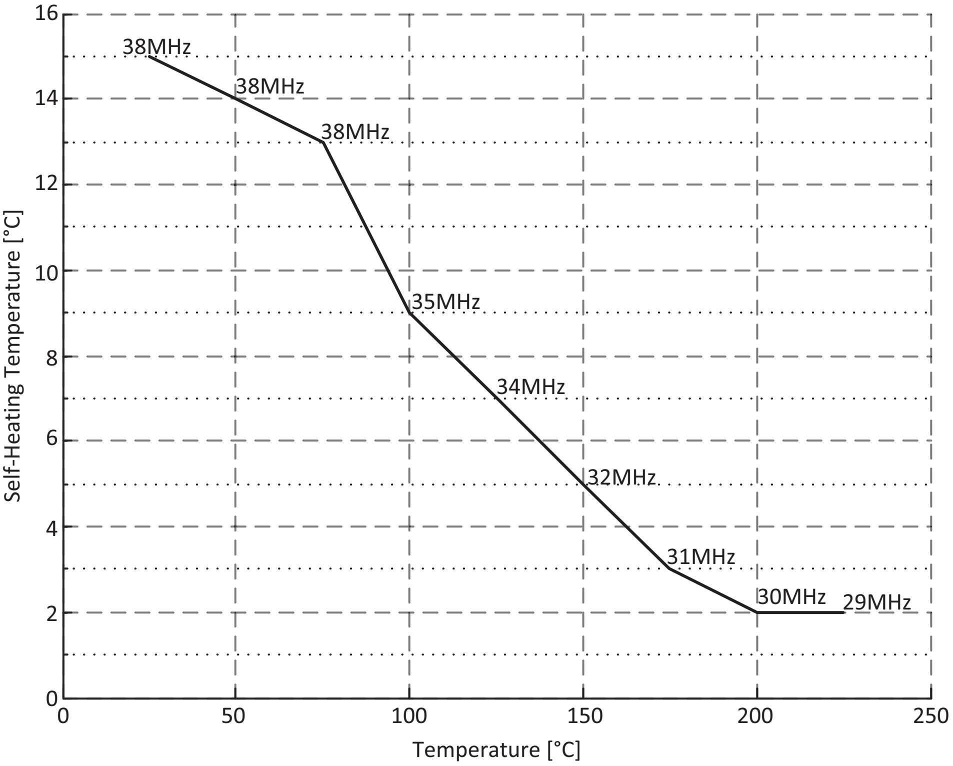


Figure 4.14: Absolute Self-Heating Values at High Temperatures.

4.5.3 Dynamic Clock Reconfiguration at High Temperatures

Based on the high temperature measurement results for the maximum operating frequency, we can identify reliable operating frequency, f_{REL}, for each associated temperature. The reliable operating frequency for a given temperature is determined by the maximum operational frequency, f_{MAX}, at 25°C higher temperature:

$$f_{REL}[T] = f_{MAX}\left[T + 25^{\circ}C\right] \tag{4.4}$$

The concept of reliable operating frequency with respect to the die temperature allows us to increase design reliability using hardware/software co-design. We propose a post-characterization algorithm that is capable of dynamical reconfiguration of the operating frequency. The reconfiguration is done such that the system operates exclusively on the reliable operating frequency at all the die temperatures.

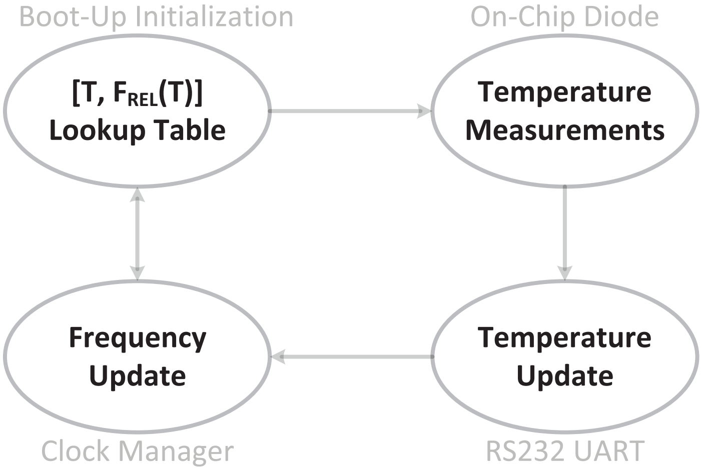


Figure 4.15: The Reliable Operating Frequency Reconfiguration Algorithm.

The reliable operating frequency reconfiguration algorithm is presented in Fig. 4.15 and the reliable operating frequencies values are presented in Table 4.2.

Table 4.2: Reliable Operating Frequencies at High Temperatures.

Temperature [°C]	f_{MAX} $[MHz]$	f_{REL} $[MHz]$
25	38	38
50	38	38
75	38	35
100	35	34
125	34	32
150	32	31
175	31	30
200	30	29
225	29	28

The reliable operating frequency reconfiguration algorithm is executed in the following steps:

- During the boot-up, the reliable operating frequency values get stored in a look-up table identical to Table 4.2.The look-up table is stored in the Data section of the SRAM. These values will be used to reconfigure the Clock Manager that is capable of changing the operating frequency dynamically.

- We repetitively perform die temperature measurements using an on-chip diode. Such two-point temperature measurements are usually processed off-chip and the result of the die temperature is communicated to a PC. The resolution of die temperature measurements is 10°C.

- Once it has been observed that the die temperature increased by 25°C, we send the new die temperature value to the Firebird SoC using the RS232 UART.

- The RS232 UART generates an interrupt that searches the look-up table. It extracts associated reliable operating frequency for the measured die temperature. The value of reliable operating frequency is forwarded to the Clock manager and the Firebird SoC continues its operation at the new operating frequency.

The reconfiguration algorithm provides reliability improvement by anticipating elevated temperature by 25°C. As described previously, this is a fully software implementation which exploits two hardware customizations: on-chip diode for temperature measurements and dynamically reconfigurable operating frequency of the Clock manager.

Further reliability improvements would assume an on-chip temperature sensor which eliminates the off-chip temperature value calculation. Such solution additionally increases the overall reliability of the system.

4.6 Conclusion

We designed, manufactured and measured Firebird, a PowerPC e200 based SoC for operation beyond 200°C. We propose to customize a PowerPC e200 based SoC by using a dynamically reconfigurable clock frequency, exhaustive clock gating, and electromigration-resistant power distribution network. Besides a powerful core and bus, the system features on-chip memories and several communication interfaces. We fabricated a 20x9 mm^2 chip implementing this design in 0.35μm Bulk CMOS process. We present world's first PowerPC based SoC for reliable operation at 225°C $(f_{MAX} = 30\,MHz,\ P_{TOT} = 1.2\,W)$, a temperature which has never been achieved by previous PowerPC based SoCs.

5 High Temperature Applications of the Time-to-Digital Conversion

This chapter is dedicated to the TDC (*Time-to-Digital Conversion*) design technique and its high temperature applications. First, we introduce this time-domain technique and reveal its strong points. After that, we exploit it for designing a DTS (*Digital Temperature Sensor*) and a Flash ADC (*Analog-to-Digital Converter*). Finally, we discuss simulation results and conclude this chapter.

5.1 Introduction

The TDC (*Time-to-Digital Conversion*) could be simply described as a technique which compares transitions of two or more signals in the time-domain. It was introduced by Ojala et Al in 1973 [60]. This technique is often used for high-time-resolution physics experiments [61], or for high-time-resolution jitter measurements [62]. For purposes of this chapter, we will reduce the TDC definition to the comparison of the propagation delays of two signals in the time-domain.

The basic TDC implementation assumes a counter that increments by every clock cycle. The current counter value represents the TDC result. Such implementation usually assume two additional digital signals, $START$ and $STOP$, which are used to initiate and end the conversion. The basic TDC operation principle is presented in Fig. 5.1.

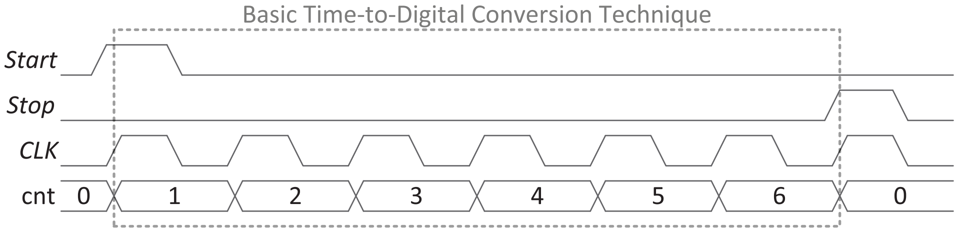


Figure 5.1: The Basic TDC Operation Principle.

All the reported techniques assume multiple clock cycles TDC. We introduce a novel TDC technique, executable in a single clock cycle.

5.1.1 Time-to-Digital Converter

There are two different implementations of the TDC, presented in Fig. 5.2, depending on which sort of the time-domain comparison is needed:

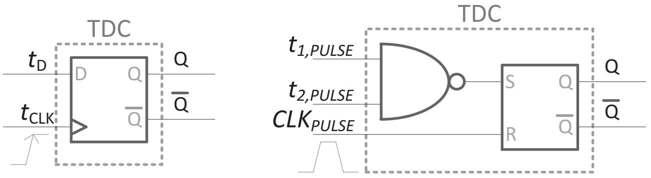


Figure 5.2: The Two Main Options for TDC Implementations.

- When the TDC compares which of the two signals transitions occurs earlier in the time-domain, a simple D flip-flop is used.

- When the TDC compares if the two voltage pulses occur at the same time, a NAND SR latch is used.

The D flip-flop is used as a TDC to determine weather t_D signal transition leads or lags the signal transition of t_{CLK}. In the case of D flip-flop, we exclusively compare rising-edges of t_D and t_{CLK} in the time-domain. The main operation principles of this TDC, implemented by a simple D flip-flop, are presented in Fig. 5.3.

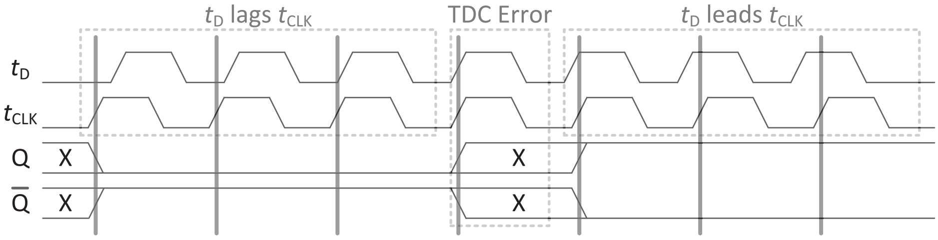


Figure 5.3: The D Flip-Flop TDC Operation Principles.

The time-domain comparison error is caused mainly by the sampling window of D flip-flop that is dominated by the hold time [63]. The time-domain difference, of two events in time we are trying to detect, is larger then the hold time for several orders of magnitude. To conclude, the TDC error introduced by D flip-flop can be neglected.

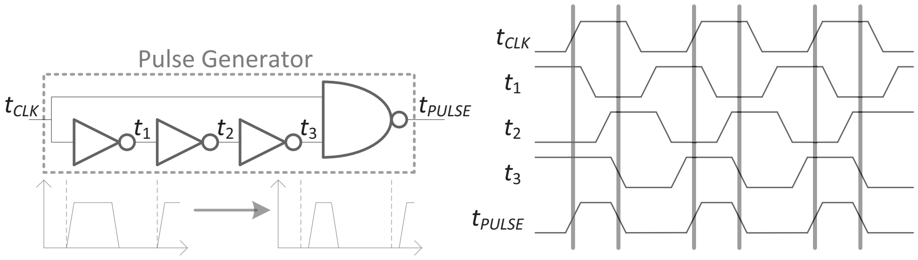


Figure 5.4: Typical Implementation of the Pulse Generator.

In order to change the time-domain comparison from rising-edges to voltage pulses, we introduce the *Pulse Generator*. A typical implementation of the Pulse generator is presented in Fig. 5.4. As it could be observed, the in input rising-edge t_{CLK} is converter to the output pulse t_{PULSE}, using a CMOS NAND logic gate and three CMOS inverters. In case a complementary output pulse t_{PULSE} is needed, the CMOS NAND should be substituted by a CMOS NOR logic gate.

The NAND SR latch is used as a TDC to determine weather $t_{1,PULSE}$ and $t_{2,PULSE}$ pulses occur at the same time. The main operation principles of this TDC, implemented by a CMOS NAND logic gate and simple SR latch, are presented in Fig. 5.5. This configuration infers a CLK_{PULSE} pulse to preserve its synchronous operation with respect to the CLK signal. As it could be observed, the CLK_{PULSE} pulse causes default Reset state ($Q =$ '0' and $\overline{Q} =$ '1').

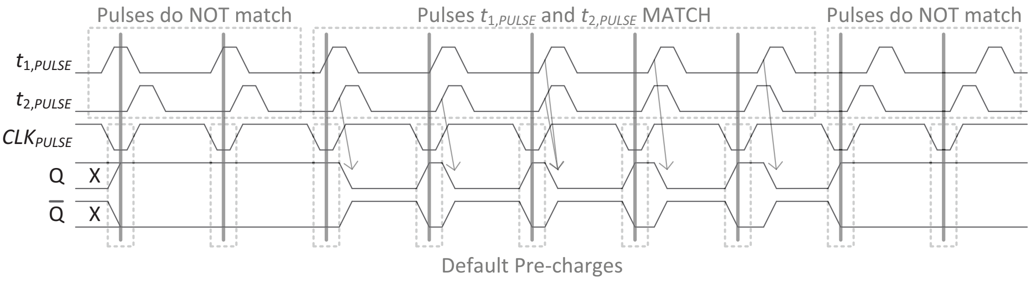


Figure 5.5: The NAND SR Latch TDC Operation Principles.

The time-domain comparison error is caused mainly by the sampling window of SR latch that is, again, dominated by the hold time. In order to reduce the joint impact of these three pulses to the hold time, we propose a novel NAND SR latch topology presented in Fig. 5.6. This topology integrates the CMOS NAND logic gate into the SR latch and reduces the overall hold time. Further, when used as a TDC, this NAND SR latch consumes less power and does not infer any time-domain comparison error.

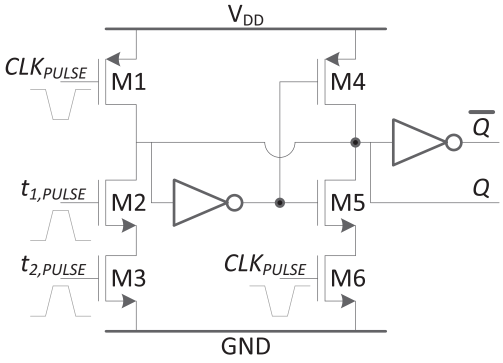


Figure 5.6: The Novel NAND SR Latch Topology.

To conclude, we present two different TDC which are used in this chapter. Depending if we compare the propagation delays of two rising-edges or voltage pulses, the D flip-flop and NAND SR latch are being used, respectively.

5.2 A Pulse Based Low-Resolution Digital Temperature Sensor

Today, complex digital SoC demand low-power high-performance, on-chip, reliable temperature sensors. Important applications of on-chip temperature sensing inside the SoC include the thermal compensation, power consumption and die temperature control [64]. In recent years, several time-domain DTS are developed for SoC applications and reported in [65], [66] and [67]. These DTS demonstrate design benefits of small area, low power, and fairly complex design effort. The basic DTS operation principle could be explained by the following two steps [68]:

- A DTS compares the propagation delay of the TDDL (*Thermally-Dependent Delay Line*) to the propagation delay of the TSDL (*Thermally-Stable Delay Line*).

- A DTS converts, using the TDC, the comparison result into a digital code.

In 2005, Pertijs et Al reported the that time state-of-the-art temperature sensor, with inaccuracy of 0.1°C (3σ) for $T_{j,MIN}$ = -55°C to $T_{j,MAX}$ = 125°C on-chip temperatures measurements. It was achieved by combining offset cancellation, dynamic element matching, curvature correction and individual trimming at room temperature after packaging [67]. However, the chip size was as large as 4.5 mm^2 in a $0.7\mu m$ CMOS process, disabling this design to be embedded into low-power high-performance SoC. The same year, Chen et Al reported on the time-domain DTS performing two-point calibration to have its accuracy approaching to that of the voltage-domain temperature sensors [66]. For reducing calibration time and efforts, a dual-DLL based DTS [65] was proposed in 2009 by Woo et Al. This design introduces the one-point calibration which removes the effects of process and supply voltage variations. However, this design infers very complex circuit topology and high power consumption, which is in the order of the mW. More importantly, this design is not a truly digital, having that it requires a power-hungry charge-pump inside the TSDL.

Thus, previously reported DTS designs are not suitable for low-resolution low-power die temperature measurements. The DTS having these characteristics are often used for the thermal compensation and die temperature control inside the SoC, as it has been presented in [69] how the power and temperature control are implemented on the $90nm$ Itanium processor by *Intel Corporation.* For instance, the threshold voltage regulation, using adaptive body-biasing technique, requires low-resolution die temperature values [70]. In order to regulate the threshold voltage, a 10°C resolution die temperature measurements in between $T_{j,MIN}$ = -45°C and $T_{j,MAX}$ = 125°C are needed. The most important requirement for the DTS is reliable operation across the whole temperature range. In this section, we present a DTS designed for the thermal management applications for the Firebird SoC [43].

5.2.1 Top Level Architecture

The design consists of three main blocks, the TDDL (*Thermally-Dependent Delay Line*), TSDL (*Thermally-Stable Delay Line*) and TDC (*Time-to-Digital Converter*). The DTS top level architecture is presented in Fig. 5.7. This design was strongly inspired by Woo et Al [65]. However, this DTS exploits original and totally novel architecture of the TSDL, which is the most important part of the DTS.

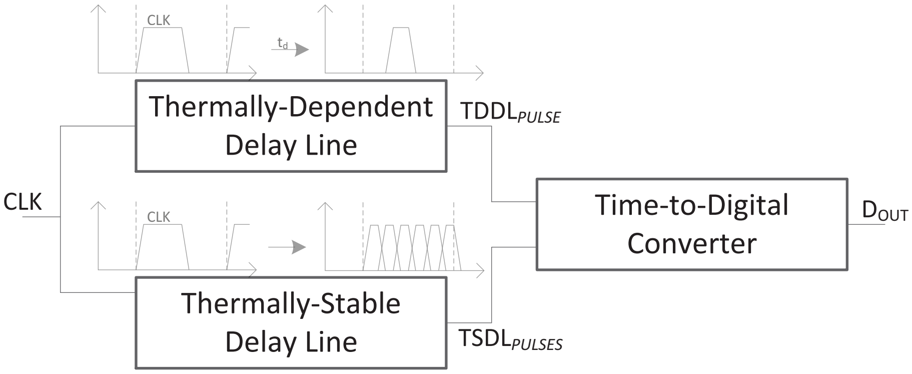


Figure 5.7: The DTS Top Level Architecture.

As presented in Fig. 5.7, the CLK signal propagates through both the TDDL and TSDL. The TDDL generates a single pulse at the output. The TDDL pulse linearly shifts it in the time-domain, due to different die temperatures which are affecting its propagation delay. The TSDL generates a family of equally delayed pulses. These pulses preserve the same propagation delays across the whole temperature range. The TDDL pulse is compared in the time-domain with the TSDL pulses, and it is done by the Time-to-Digital convertor. The digital output code of the TDC is registered and it represents the value of measured die temperature.

5.2.2 Thermally-Dependent Delay Line

As we previously mentioned, the TDDL pulse shifts in time-domain with respect to the die temperature: lower the die temperature, the TDDL pulse propagation delay decreases, and higher the die temperature, the TDDL propagation delay increases. The TDDL consists of a simple CMOS inverter chain, equivalent to one presented in the Chapter 1. For this design, we used the minimum feature CMOS inverters, having that these CMOS logic gates are the most sensitive to the thermally-caused effects.

The TDDL must be sufficiently long, so that the elevated temperatures cause significant propagation delay difference caused by the 10°C die temperature shift. This is the only design challenge when determining the length of TDDL.

The TDDL is very sensitive to process variations. They affect the propagation delay the same way the thermally-caused effects do. Such behavior is expected, but these two mutually-exclusive sources of the propagation delay shifts must to be separated by design. That is why this design needs a calibration step. The calibration step must be done at the known temperature. Based on the calibration result, the TDDL propagation delay has to be trimmed such that the process variations effect is canceled out. For the trimming purpose, a simple CMOS multiplexer could be used. The TDDL architecture is presented in Fig. 5.8.

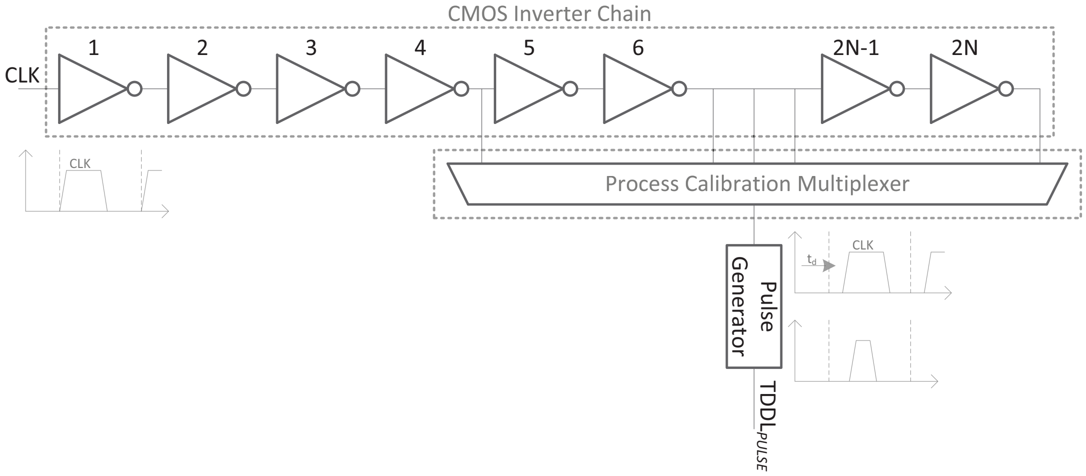


Figure 5.8: The TDDL Architecture.

5.2.3 Thermally-Stable Delay Line

The TSDL is the essential part of the DTS. It generates equally delayed pulses used to match the propagation delay of the TDDL pulse in the time-domain. The TSDL must preserve propagation delays of its pulses across the whole temperature range.

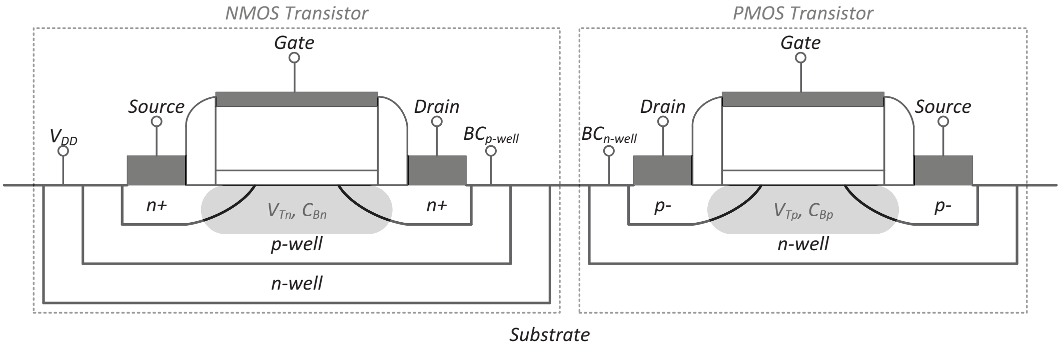


Figure 5.9: The CMOS Inverter Cross-Section.

We propose a novel TSDL architecture which exploits the threshold voltage, V_T, regulation using the ABB (*Adaptive Body-Biasing*) technique. In order to preserve the constant propagation delays of the TSDL pulses across the whole temperature range, the V_T is regulated in the closed-loop feedback configuration. The main regulation principle is to manipulate the body-bias of the *n-* and *p-well* of the PMOS and NMOS transistors, respectively. As the die temperature increases, the V_T should be decreased, so that the MOS transistor gets additional overdrive voltage, (V_{GS} - V_T). Similarly, when the die temperature decreases, the V_T should be increased, so that the overdrive voltage reduces. We will analyze the threshold voltage V_T and associated overdrive voltage (V_{GS} - V_T) regulation on the example of a CMOS inverter. A CMOS inverter cross-section is presented in Fig. 5.9, where the equivalent well capacitances, C_{Cp} and C_{Cn}, are highlighted.

The regulation of threshold voltages, V_{Tn} and V_{Tp}, is performed using the MOS transistor body-contacts, BC_{p-well} and BC_{n-well}. Thus, in order to increase or decrease the threshold voltage, the well capacitances C_{Bp} and C_{Bn} have to be charged or discharged. There should be a current running through the body-contacts BC_{p-well} and BC_{n-well} which charges and discharges the well capacitances C_{Bp} and C_{Bn}. This current will be used as the regulation variable that directly impacts the threshold voltages, and indirectly, the propagation delays of the CMOS inverters. Regulation circuit consists of a time-domain comparator that drives switches to charge and discharge well capacitances C_{Bp} and C_{Bn}. The time-domain comparator pulses decide if the CMOS inverter should increase or decrease its propagation delay.

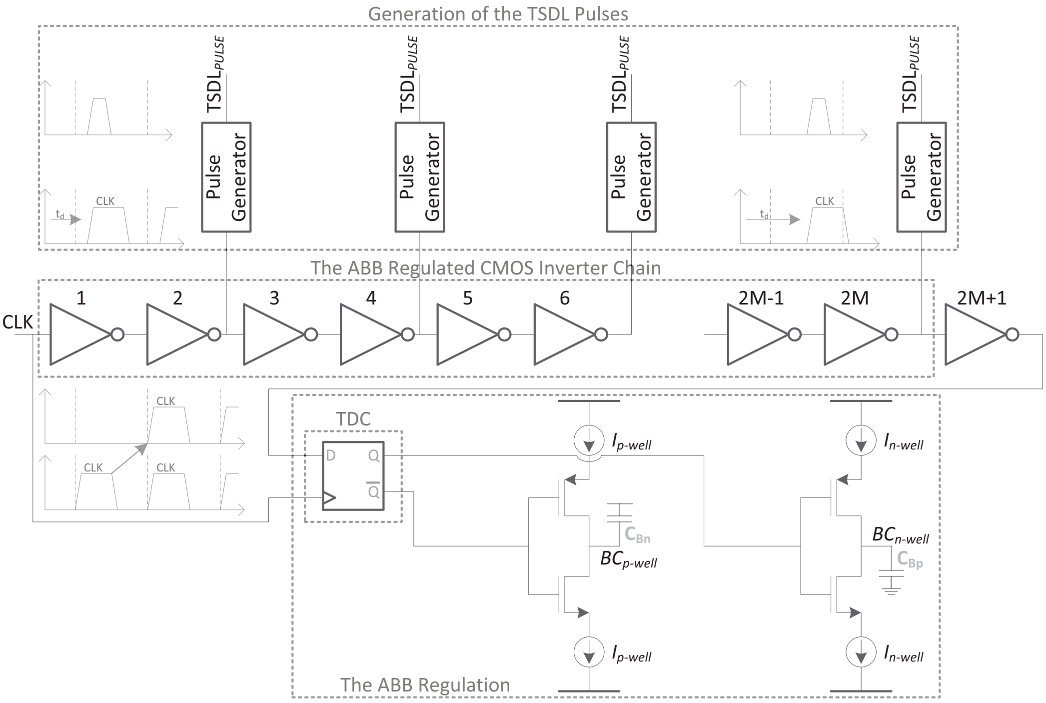


Figure 5.10: The TSDL Architecture.

Once we establish control of propagation delays of a CMOS inverter across the whole temperature range, we may exploit this concept to design the TSDL. Essentially, the TSDL family of equally delayed pulses are generated in the first half-period of the input clock signal, CLK. The CLK falling-edge arrival in the time-domain is compared with the propagation delay of CMOS inverter chain, that is regulated using the ABB technique.

If the CMOS inverter propagation delay arrives earlier, in the time-domain, then CLK falling-edge, then the CMOS inverter chain should increase its propagation delay. On contrary, if the CMOS inverter propagation delay arrives latter, in the time-domain, then CLK falling-edge, then the CMOS inverter chain should decrease its propagation delay. The TSDL architecture, including the regulation circuit, is presented in Fig. 5.10.

In order to charge and discharge the well capacitances C_{Bp} and C_{Bn} such that the threshold voltages V_{Tn} and V_{Tp} are increased and decreased for the same value, the currents, I_{p-well} and I_{n-well}, running through the body-contacts BC_{p-well} and BC_{n-well} must satisfy the following equation:

$$\frac{I_{p-well}}{C_{Bn}} = \frac{I_{n-well}}{C_{Bp}} \Rightarrow \frac{I_{p-well}}{W_n} = \frac{I_{n-well}}{W_p} \tag{5.1}$$

Having that the well capacitances C_{Bp} and C_{Bn} are directly proportional to the WxL for both the NMOS and PMOS transistors, the ratio of the C_{Bp} and C_{Bn} is equal the ratio of the NMOS and PMOS transistor widths W_n and W_p.

The ABB regulation is sampling limited to the resolution of the TDC, which is, in this case, implemented using a D flip-flop. The sampling error, introduced by the hold time of the D flip-flop, does not impact TSDL operation and system stability.

Further, such implementation of the TSDL is inherently immune to process variations. As previously mentioned for the TDDL, process variation affect the propagation delay of the CMOS inverter chain the same way the thermally-caused effects do. The closed-loop feedback ABB regulation preserves the propagation delay of the CMOS inverter chain for the whole temperature range and across the process corners.

5.2.4 Conclusion

In this section, we propose a novel DTS architecture that could be used for the SoC thermal management applications.

This design has been successfully demonstrated with Flash Design Team, Memory Division, Samsung Electronics.

We do not provide any simulation or measurement results in this section, because of the mutual NDA (*Non-Disclosure Agreement*). The TDDL and TSDL sizing depends on the operating frequency, supply voltage, MOS transistors properties, process parameters and layout rules. For the purpose of this section, we only presented our contribution to the TDC principles and DTS implementations.

5.3 A Pulse Based Flash Analog-to-Digital Converter

Modern SoC are increasing their demand for power-efficient high-performance ADC. There are many important applications of A/D conversion in modern SoC, which span from reading analog outputs from off-chip sensors in temperature and voltage sensing applications [71], to high frequency serial receivers in communication applications [72]. In 2013, there were several Flash ADC implementations, reported in [73], [74] and [75], which demonstrate state-of-the-art power-efficiency of approximately 100 fJ/conv. These Flash ADC also demonstrate design benefits of small area, low power, and fairly complex design effort.

The basic Flash ADC was introduced by Charles E. Woodward in 1975 [76]. This early report on a 3bit Flash ADC describes its operation principles which remain valid as of today. The main A/D conversion concept could be explained by the following two steps:

- A resistive ladder generates reference voltage levels, which are used as the quantization levels for the A/D conversion.

- Input analog voltage is then compared with the reference voltage levels, resulting by a 1bit digital value for each quantization level.

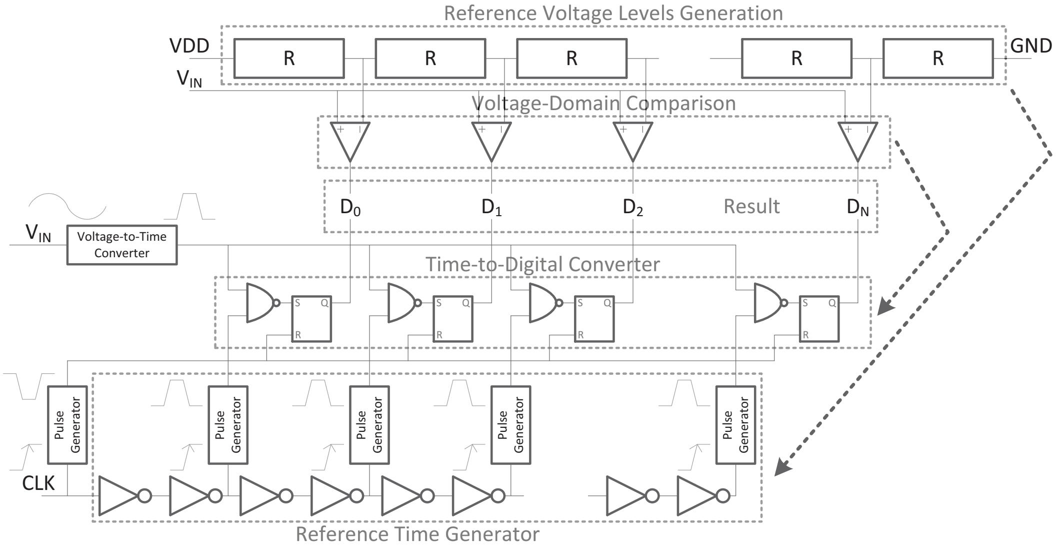


Figure 5.11: Transition from Voltage- to the Time- Domain.

The main idea of this work is to replace voltage- to the time-domain comparison, by applying the following customizations to the conventional Flash ADC architecture:

- The resistive ladder is substituted by RTG (*Reference Time Generator*) which generates reference pulses in the time-domain. These pulses are used as the quantization levels.

- Input analog voltage also converted to the time-domain pulse, using the VTC (*Voltage-to-Time Converter*). This VTC pulse is then compared with the RTG pulses using the TDC technique, which results by a 1bit digital value for each quantization level.

As for the proof of concept, this section demonstrates the Pulse based Flash ADC designed for the room temperature operation. The concept of voltage- to time-domain operation transfer is presented in Fig. 5.11.

This design exploits the same TDC technique that is used for the DTS design. Thus, as previously presented in this chapter, the pulse based TDC is performed using dedicated NAND SR latches.

On contrary, the VTC and RTG blocks are designed and sized specially for this Flash ADC. Their architectures and operation principles are subject of discussion in the following two subsections.

5.3.1 Voltage-to-Time Converter

The Voltage-to-Time conversion is needed for the time-domain representation of the analog input signal, V_{IN}. VTC converts the input voltage into the time-domain pulse, following a single rule: higher the input voltage V_{IN}, shorter the propagation delay of the VTC_{PULSE} pulse. Counter-wise, lower the input voltage V_{IN}, longer the propagation delay of the VTC_{PULSE} pulse.

In order to achieve such functionality, we implemented VTC using the S&R (*Sample & Ramp*) technique. The S&R design approach consists of two steps, described by [77]:

- Sample: This step assumes sampling input voltage and preserving the sample value to be used during the conversion

- Ramp: Once sampled, the input voltage value is linearly increased for the constant time of a clock cycle

Once obtained by these two steps, the S&R voltage $V_{S\&R}$ is compared to the constant referent voltage V_{REF}. Essentially, this is how the time is introduced and associated with the input voltage V_{IN}. The VTC implementation using a S&R circuit is presented in Fig. 5.12.

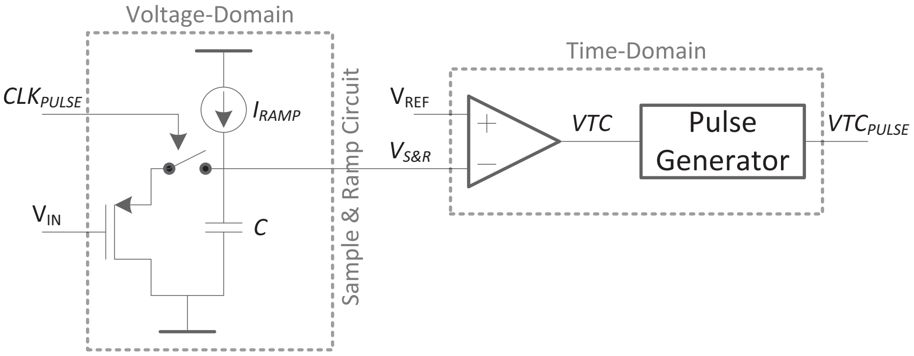


Figure 5.12: The VTC Architecture.

As it could be observed, the sampling occurs when the CLK_{PULSE} activates the transmission gate switch. The analog input voltage is applied to a source-follower, defining the initial value for the $V_{S\&R,0}$:

$$V_{S\&R,0} = V_{IN} + V_{SG} \tag{5.2}$$

where V_{SG} is the *Source* to *Gate* voltage of the PMOS transistor. Further, when the time t is included into previous equation, we get the following time-dependent equation for the $V_{S\&R}$:

$$V_{S\&R} = V_{S\&R,0} + \frac{I_{RAMP}}{C} t \tag{5.3}$$

where the the I_{RAMP} is the constant current which generates voltage $V_{S\&R}$ over the input capacitance C. Once the $V_{S\&R}$ reaches referent voltage V_{REF}, comparator output generates a rising-edge of signal VTC, that is a time-domain representation of the input voltage V_{IN}. Finally, the propagation delay of the VTC could be described by the following equation:

$$t_{RAMP} \approx \frac{C}{I_{RAMP}}(V_{REF} - (V_{IN} + V_{SG})) \Rightarrow t_{RAMP} = -\frac{C}{I_{RAMP}} V_{IN} + V_{const} \tag{5.4}$$

Thus, the propagation delay t_{RAMP}, that will be used for the TDC, is directly proportional to the input voltage V_{IN}. The VTC operation principle and VTC_{PULSE} pulse generation are presented in Fig. 5.13.

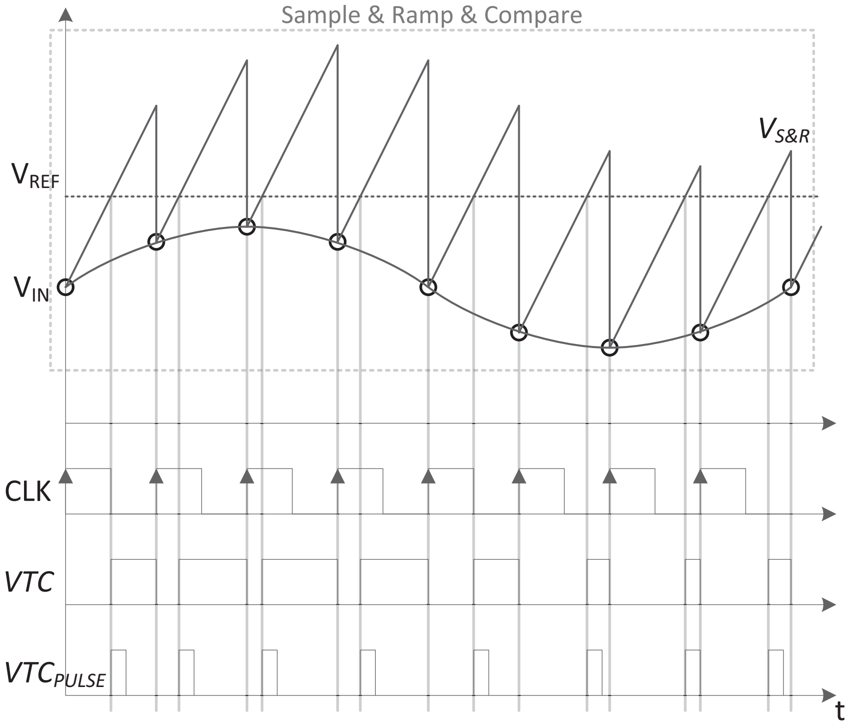


Figure 5.13: The VTC Operation Principles.

5.3.2 Reference Time Generator

The RTG generates equally delayed pulses, RTG_{PULSES}, used to match the propagation delay of the VTC_{PULSE} pulse in the time-domain. These pulses are used as the quantization levels of this Flash ADC. The time-domain reference generation is presented in Fig. 5.14.

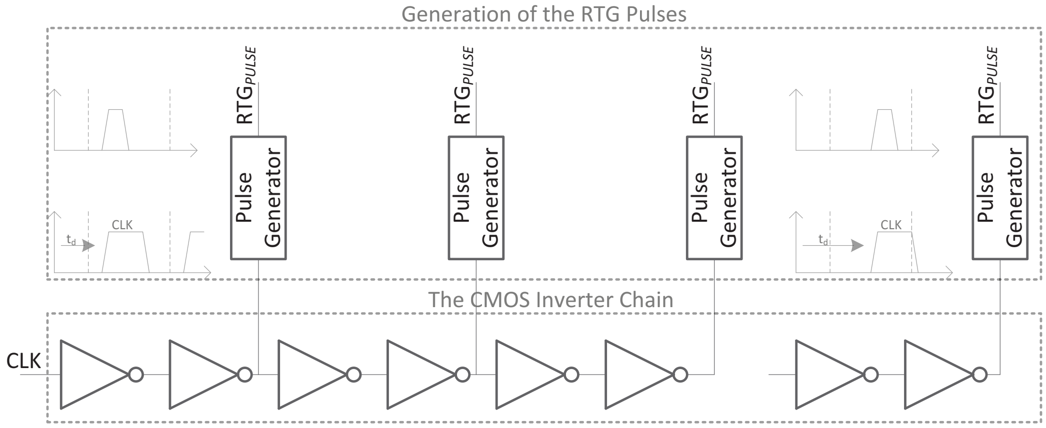


Figure 5.14: The RTG Architecture.

The VTC_{PULSE} pulse varies its propagation delay with respect to the input voltage V_{IN} value. Thus, the RTG_{PULSES} pulses must provide referent time that is used to match VTC_{PULSE} pulse propagation delay. Once there is a match in time-domain, it is recognized by the NAND SR latch that does the T/D conversion. The digital value of the NAND SR latch TDC, 5bit $D[4:0]$ in this case, is the result of the A/D conversion. The RTG operation principles with respect to the VTC are presented in Fig. 5.15.

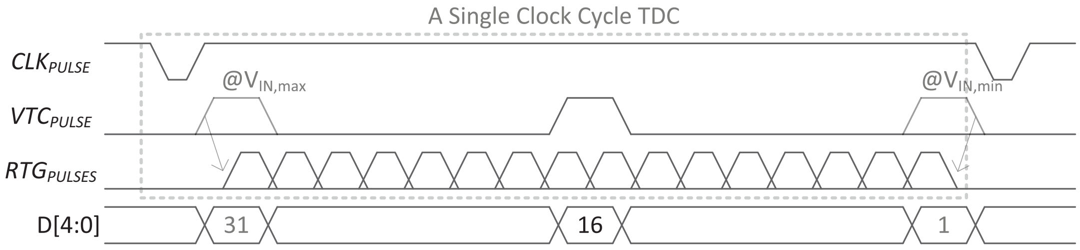


Figure 5.15: The RTG Operation Principles.

As it could be observed, the TDC results by 5bit digital values, $D[4:0]$. The RTG generates sixteen pulses which match the VTC pulse, but matching occurs in two different manners:

• First, there is a case when the VTC_{PULSE} matches with a single RTG_{PULSE} in the time-domain. In that case, only one NAND SR latch changes its state to Set, asserting its outputs to ($Q =$ '1' and $\overline{Q} =$ '0').

•Second, there is a case when the VTC_{PULSE} matches with two RTG_{PULSE} pulses in the time-domain. When this is the case, two NAND SR latches instantly change their states to Set.

This hybrid one-hot coding scheme is constructed exclusively for this design and, to the best of our knowledge, it has not been previously reported. Such coding scheme is achieved by sizing widths of the VCT and RTG pulses as:

$$W(VTC_{PULSE}) = 1.5 \times W(RTG_{PULSE}) \tag{5.5}$$

The 5bit HOH (*Hybrid One-Hot*) coding scheme is presented in Table 5.1. Such coding scheme allows us to use only sixteen RTG_{PULSES} and NAND SR latches to obtain thirty two quantization levels A/D conversion. As for the comparison, the conventional Flash ADC architecture assumes equal number of comparators to the number of reference voltage levels and it exclusively relies on the thermometer coding scheme. Further, conventional Flash ADC require additional error-correction logic that is used to prevent from bubbles in the thermometer coding scheme, as presented in [78].

Table 5.1: The Hybrid One-Hot Coding Scheme.

NAND SR Latches States	$D[4:0]$	Decimal Value
1111111111111111	00000	0
1111111111111110	00001	1
1111111111111100	00010	2
1111111111111101	00011	3
1111111111111001	00100	4
1111111111111011	00101	5
1111111111110011	00110	6
...	...	...
1001111111111111	11100	28
1011111111111111	11101	29
0011111111111111	11110	30
0111111111111111	11111	31

5.3.3 Design Summary

Presented Pulse based Flash ADC is a scalable architecture. Inherent scalability of the Flash ADC could be described by following statement: If the Flash ADC resolution is to be increased for a single bit, the reference voltage levels and comparators number must be doubled. Thus, the Flash ADC resolution must be chosen carefully in order to obtain power-efficient design [79]. The mainstream ENOB (*Effective Number Of Bits*) for the modern Flash ADC is 5bit and this design is sized accordingly.

We implemented this Pulse based Flash ADC in standard $0.18\mu m$ CMOS process. When sizing this Flash ADC, we must take into account the operating frequency, supply voltage and process variations. First, we define the RTG pulses width to $t_{RTG} = 200\ ps$ for $1.8\ V$ supply voltage and typical process corner, TT. Based on that, the VTC pulse width is defined to $t_{VTC} = 300\ ps$, taking into account that it should be one and a half times the RTG pulse width.

Referring back to the Fig. 5.15, the CLK period is defined by following relation:

$$T_{CLK} = 2 \times (16 \times t_{RTG} + t_{VTC} + t_{CLK}) \approx 2 \times (16 \times t_{RTG} + 2 \times t_{VTC}) \tag{5.6}$$

where the CLK pulse width t_{CLK} is approximated to the VTC pulse width, $t_{CLK} \approx t_{VTC} = 1.5 \times t_{RTG}$. This computation sizes the CLK period to $10\,ns$ for the nominal $1.8\,V$ supply voltage and typical process corner, TT. Fast and slow process corners, FF and SS, cause the time-domain pulses to shrink and expand, respectively. As a consequence, the quantization levels change their absolute values but they preserve their relative ratio. The FF and SS fabrication outcomes could be easily compensated by the V_{REF} and I_{RAMP} adjustments.

The design implementation microphotograph is presented in Fig. 5.16. The silicon area occupied by this design is $130\,\mu m \times 73\,\mu m$.

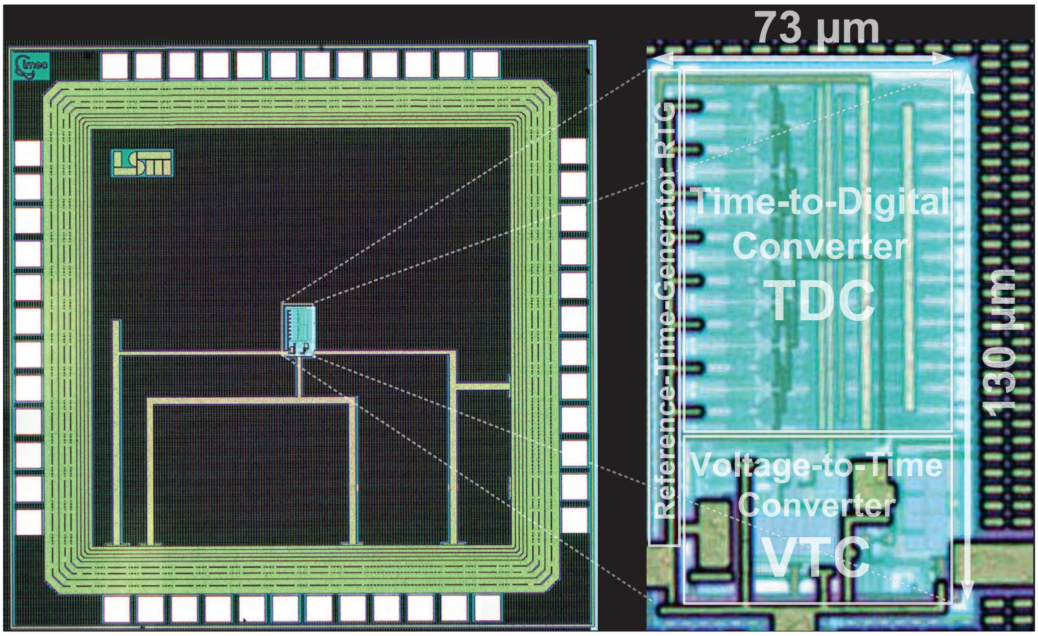


Figure 5.16: The Pulse Based Flash ADC Microphotograph.

One of the strongest implementation features of this design is its small silicon area. Taking into account its digital nature, we characterized this area result the way it is done for digital systems. Thus, we compare this Flash ADC area with the area of a minimum driving strength two-input NAND CMOS logic gate implemented in $0.18\mu m$ CMOS process ($5.44 \times 1.86\,\mu m^2$). This comparison results by a 1kGate, meaning that this design occupies silicon area equal to the thousand NAND logic gates. This is a extremely desirable result for modern digital SoC which usually occupy silicon area that is measured in 100kGate [43].

5.3.4 Simulation and Measurement Results

As previously discussed, the FF and SS process corners cause time-domain pulses to shrink and expand, respectively. On one hand, the FF process corner decreased the pulse widths by approximately 10%, resulting by new value of the t_{RTG} = 180 ps. On the other hand, the SS process corner increases the widths by approximately 20%, resulting by new value of the t_{RTG} = 240 ps. The effect of global process variations is presented in Fig. 5.17.

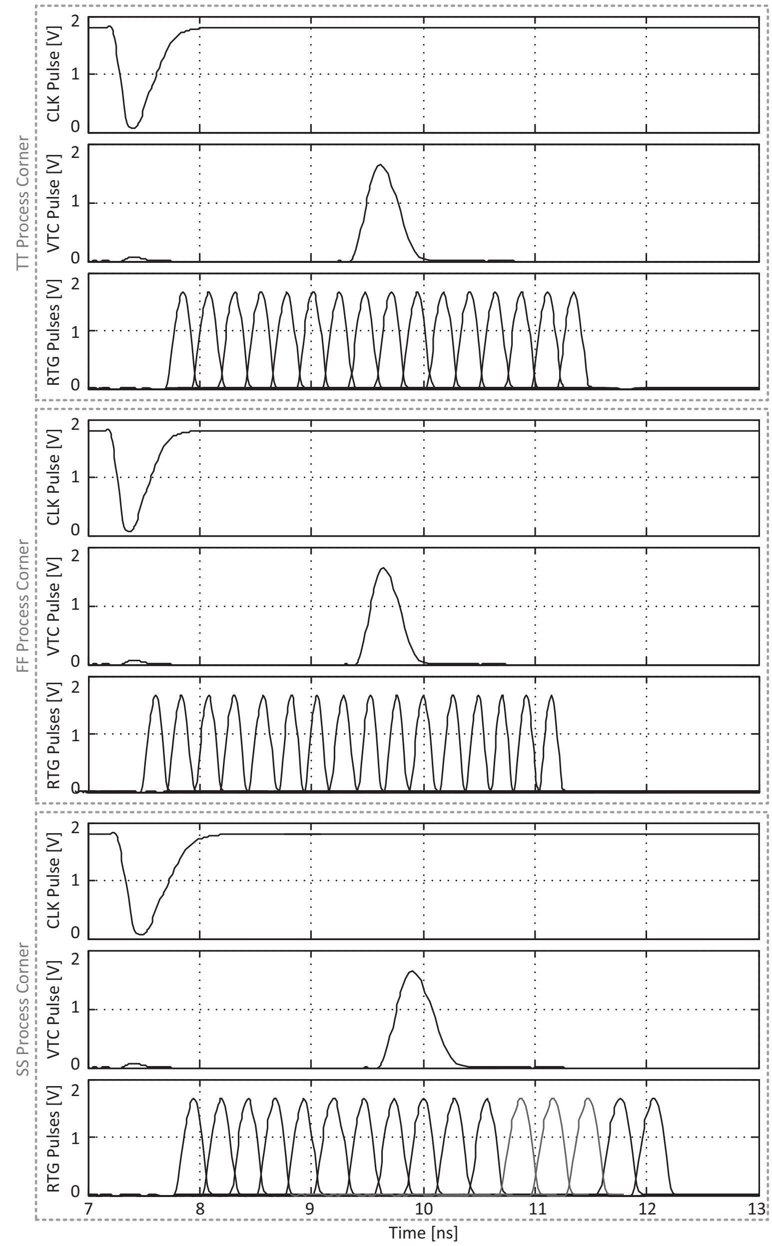


Figure 5.17: The Effect of Global Process Variations.

The local process variations, essentially the device mismatch, could cause much more serious problems comparing to global process variations described by the FF and SS. These fabrication imperfections usually impact the ADC transfer function and might affect ADC performance, such as the conversion resolution, INL (*Integral-Non-Linearity*) and DNL (*Differential-Non-Linearity*). The effect of local process variations to the ADC transfer function is presented in Fig. 5.18, based on the 20 Monte-Carlo *Spectre* simulations.

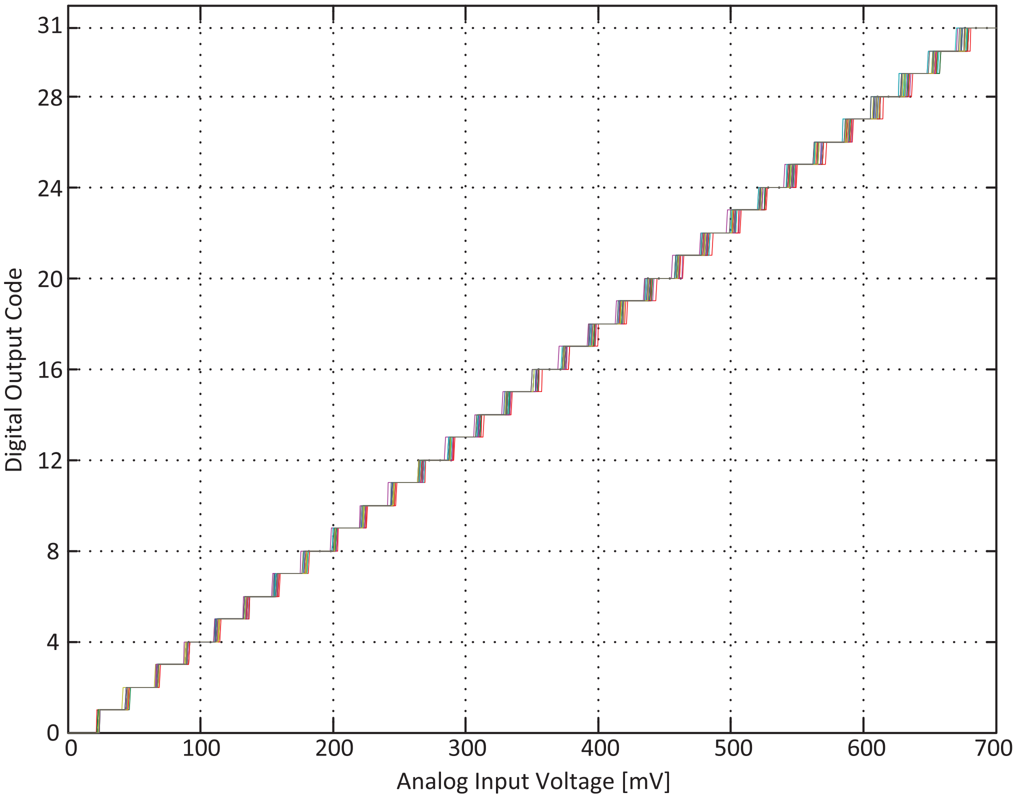


Figure 5.18: The Effect of Local Process Variations.

As it could be observed, the introduced conversion error is much lower comparing to the quantization levels and we can draw the conclusion that this Pulse based Flash ADC architecture is inherently robust to the device mismatch. For the design implementation in $0.18\mu m$ CMOS process, even the minimum size CMOS inverters provide desired timing of the $t_{RTG} = 200\ ps$, providing sufficient robustness to the local variations. The actual RTG implements two times larger transistor features, $W/L = 2W_{min}/2L_{min}$, mainly for the additional improving of the robustness to the device mismatch.

Further, the dynamic simulations have resulted by the 4.83bit ENOB, with SNR (*Signal to Noise Ratio*) and SNDR (*Signal to Noise and Distortion Ratio*) equal to 31.5 dB and 30.7 dB, respectively. The normalized output spectrum (-3 $dBSF$) of the 8 MHz input signal is presented in Fig. 5.19. The input voltage V_{IN} oscillates around 350 mV DC with the amplitude of 250 mV.

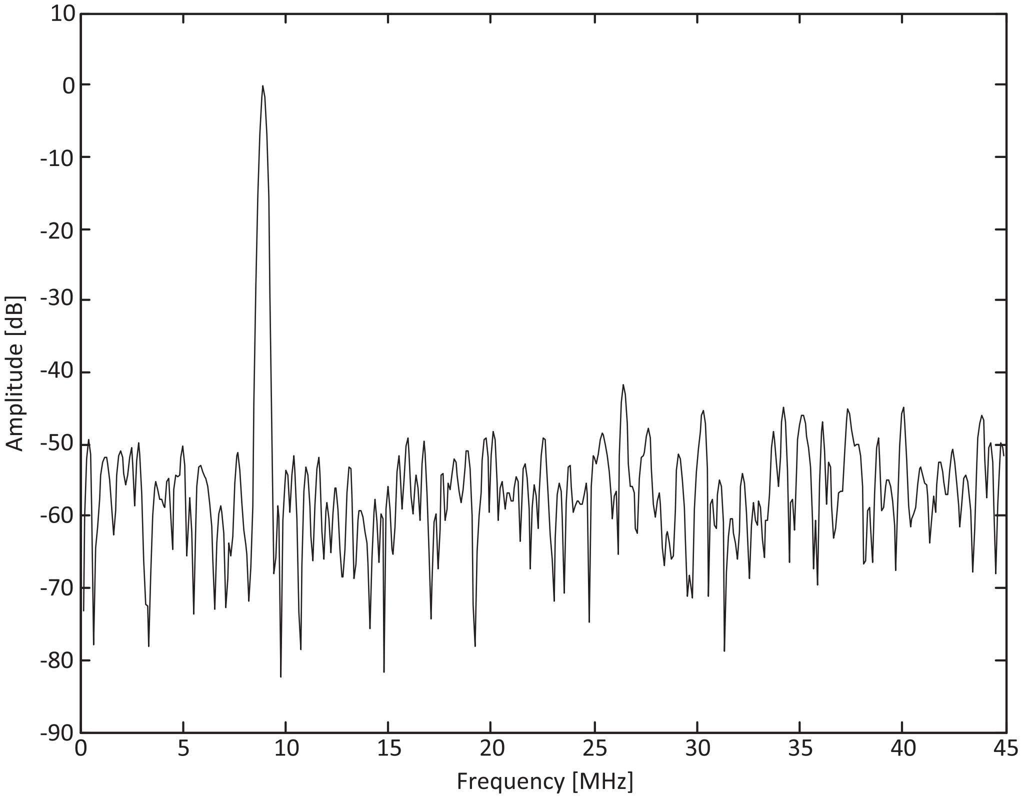


Figure 5.19: Spectrum of 8.18 MHz Input Signal at 83 MHz Sampling Rate.

The complete Pulse based Flash ADC performance summary is presented in Table 5.2. The full-scale analog input voltage V_{IN} is 0 V to 0.7 V and the nominal supply voltage is 1.8 V. It achieves the sampling rate of 83 MHz, with the power consumption of 900 mW.

Table 5.2: The Pulse Based Flash ADC Performance Summary.

Characteristics	Values
Input Range	0-700 mV
Sampling Frequency	83 MHz
Input Bandwidth	41.5 MHz
SNR	31.5 dB
SNDR	30.7 dB
Power Consumption	900 μW
Power Efficiency	450 fJ/conv
Silicon Area	130 × 73 μm^2
Process	0.18μm Standard CMOS

In order to compare this work with the state-of-the-art Flash A/D converters, we must first calculate the power-efficiency indicator, the FoM (*Figure of Merit*), defined by following equation:

$$FoM = \frac{P_{ADC}}{2 \times f_{BW} \times 2^{ENOB}} \tag{5.7}$$

where P_{ADC} is the total power consumption, $ENOB$ is the effective number of bits and f_{BW} is the input bandwidth of an ADC. When we apply the values presented in Table 5.2, this design results by the $FoM \approx 450\, fJ/\text{conv}$.

This result should be treated as the state-of-the-art achievement, especially after taking into account that it was implemented in the $0.18\mu m$ CMOS process. Newer technology nodes would definitely bring better performance in terms of the power-efficiency. The comparison with the recently reported high-performance Flash ADC is presented in Table 5.3.

Table 5.3: The State-of-the-Art Flash ADC Comparison

	Process [nm]	VDD [V]	$ENOB$ [bit]	BW [MHz]	Power [mW]	Efficiency [fJ/conv]
[80] TCAS-II 2008	90	1	6.5-7	650	207	1400
[81] Symp-VLSI 2008	90	1	3-4.8	2000	7.60	150
[82] CICC 2008	90	0.6-1	4.08-4.45	30-300	1.30-6.70	490-1060
[83] CICC 2008	180	3-3.6	4.5	6500	3300	11000
[84] JSSC 2009	90	1	4.7	878	2.20	50
[85] TVLSI 2010	130	1.2	4.54	600	120	3070
[86] Symp-VLSI 2009	65	1.1	3.9	3750	52	490
[87] JSSC 2009	130	1.2	4-5	20000	4800	11200
[88] TCAS-I 2010	65	1	4.4	700	1.97	116
[89] TCAS-II 2010	90	1.2-2.5	3.22-3.75	2500	86	1320
[90] A-SSCC 2010	90	0.5	4.2	200	1.20	160
[91] A-SSCC 2010	65	1	4.7	1500	36.20	600
[92] JSSC 2011	65	1.1	3.9	6000	81	350
[93] JSSC 2013	65	1	4.8	630	0.60	17
This Work	180	1.8	4.83	40	0.90	450

5.3.5 Conclusion

In this work, we introduced a novel time-domain operation principle using the voltage pulses. The fully-digital Pulse based Flash ADC performs a novel T/D conversion, executable in a single clock cycle. The simulation results indicate excellent power-efficiency of only $450\, fJ/\text{conv}$. In the parallel to that, the design implementation occupies fairly small silicon area that is equivalent to a 1kGate. Finally, this design shares extreme scalability that is inherent for the Flash A/D converters family. It would significantly improve its performance if implemented in a newer technology node.

5.4 Future Work

In this chapter we present a DTS for operation at high temperatures and a Pulse based Flash ADC for operation at room temperature. However, when both implemented in the same SoC, these two modules could be customized to operate at the elevated temperatures. Essentially, the die temperature measurement results, provided by the DTS, could be used to cancel out the thermally-caused effects on the VTC operation. Hence, we propose to integrate both the DTS and Flash ADC on the SoC, in a configuration where the DTS is used for the Flash ADC recalibration at the high temperatures. The integral architecture is presented in Fig. 5.20.

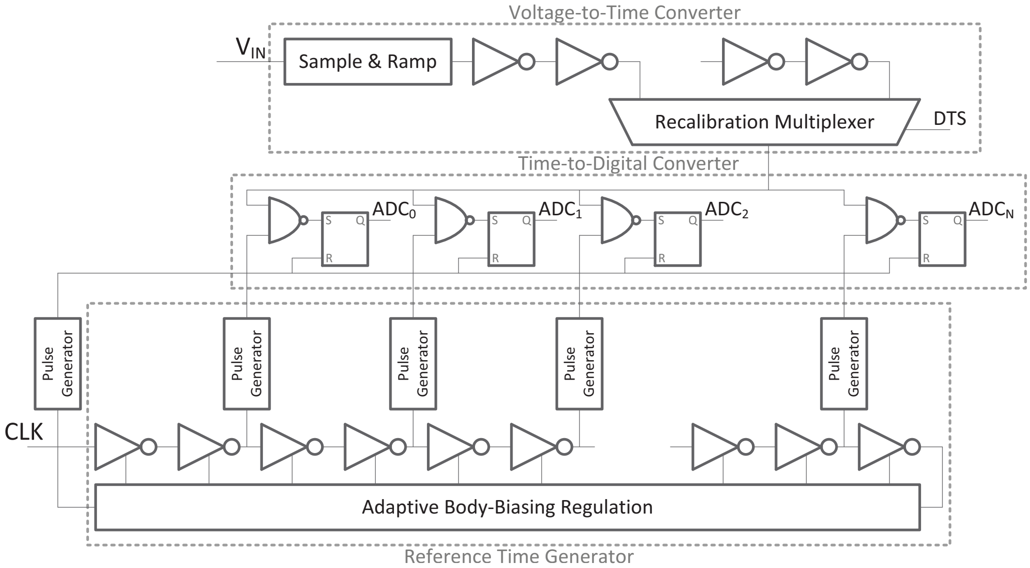


Figure 5.20: Integral DTS and Flash ADC Topology for SoC.

The two modules share the reference time generator, RTG_{PULSES}, having that both topologies need the reference pulses for the time-domain conversion. The analog input voltage time-domain representation suffers from the thermally-caused changes of the delay propagation. Thus, the main idea is to use die temperature value to manipulate the VTC operation such the thermally-caused effects are being canceled out. The recalibration consist of applying reconfigurable delay to the initial propagation delay of the VTC_{PULSE}. Lower the die temperature, more the additional delay is applied, and, counter-wise, higher the die temperature, less additional delay is applied. This solution could eventually lead to the first Flash ADC implementation for reliable operation at high temperatures.

5.5 Conclusion

In this chapter, we introduced a novel T/D conversion, executable in a single clock cycle. This operation principle is exploited to design fully-digital DTS and Flash ADC. These designs demonstrate state-of-the-art performance and prove that the Time-to-Digital conversion is a powerful design technique for improving SoC reliability.

6 Measurement and Test Techniques for High Temperature SoC Applications

This chapter is dedicated to the custom measurement and test techniques which could be used for high temperature experiments. First, we introduce the conventional high temperature ovens and discuss on their scope of application for the SoC testing. After that, we introduce the micro-heater based test setups and explain how to use them for the high temperature measurements. Finally, we discuss measurement results and conclude this chapter.

6.1 Introduction

The high temperature ovens are being used for the scientific experiments since a very long time. Conventional ovens provide a high temperature chamber with hot air flow. Air is been heated up by a heating element and circulated throughout the chamber using a fan, powered by an electric motor. Described configuration typically infers the thermocouple actuated microcontroller based digital control mechanism. A typical operating principle of the conventional high temperature ovens is presented in Fig. 6.1. The described concept is used for the *Grieve AA-1250* product.

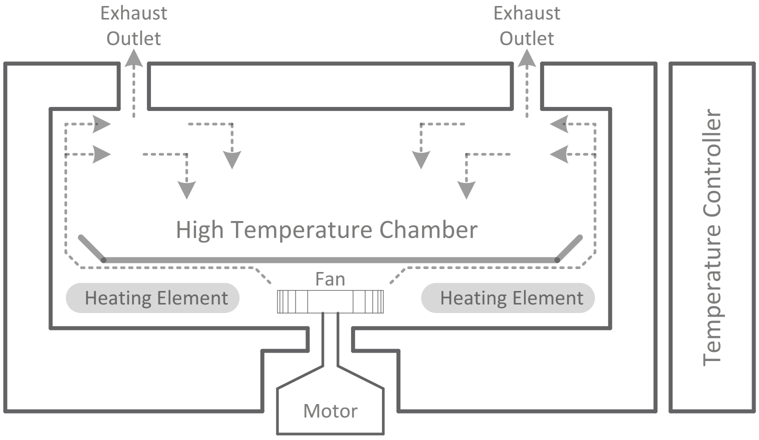


Figure 6.1: Operating Principle of the High Temperature Ovens.

Commercially available high temperature ovens are compared in Table 6.1. Maximum operating temperature (T_{MAX}), temperature-control error (T_{ERR}), heating time interval (t_{HEAT}) and controller type information of the aforementioned products, are taken from product datasheets.

Table 6.1: Comparison of the State-of-The-Art High Temperature Ovens.

Model	AA-1250	PN200	HT445	HT125	LAC 1-38A
Manufacturer	Grieve	Carbolite	JPW Design	Genlab	Despatch
T_{MAX} [°C]	677	300	594	400	260
T_{ERR} [°C]	13	7	10	-	-
t_{HEAT} $[min]$	88	52	-	-	-
Controller Type	μC	PID	Yokogawa UT150L	μC	μC

The main problem when using conventional high temperature ovens, besides the high cost, is lack of interfacing to the inside of the high temperature chamber. Limited access to the high temperature chamber reduces cabling capabilities which are needed for the complex SoC measurements and testing. As for the reminder, the silicon implementations presented in previous chapters assume hundreds of I/O pins and they require fairly complex interface with the testing equipment.

If we take a look more into details, there are serious obstacles to insert an electrical test-bench into a high temperature chamber. First of all, each electrical test-bench relays on the PCB (*Printed Circuit Board*), which mechanically supports and electrically connects the electronic components. In order to be inserted in the high temperature chamber, the PCB cannot be made of mainstream substrate FR4 (*Fiberglass-Epoxy Laminate*), having that it cannot be used at high temperatures [94]. New substrates, resistant to the high temperatures, should be used instead the FR4, namely the LTCC (*Low Temperature Co-fired Ceramics*) [95]. Thus, measurements which are conducted in high temperature ovens require special PCB materials [96].

Finally, the most important limitation for using high temperatures ovens comes from their operation principle. Their operation assumes the isothermal chamber conditions. When looking at this thermal characteristic from the electrical point of view, it draws a conclusion that all the electrical components on the test-bench must be capable of the operation at high temperatures. Hence, not only the DUT (*Design Under Test*), but also the surrounding electronic components must also be capable of reliable operation at high temperatures. The main components, among the others, are the clock oscillator, DC/DC converter, and off-chip memories.

Thus, there is an urgent demand for novel, DUT oriented, measurement and test techniques. In this chapter we propose to exploit the COB (*Chip-On-Board*) technique, combining it with regulated heating element, to achieve a low-cost high-precision thermally-controlled test-bench.

6.2 The Chip-On-Board Based Micro-Heater Test Setups

In this section we present the micro-heater[1] design, based on a miniature ceramic cantilever. The cantilever design incorporate two heaters integrated into the cantilever surface. The primary heater is used for heating the area directly under the die to the desired temperature, and the guard heater is used for ensuring that the temperature under the die is uniformly matching the temperature of the primary heater. Such configuration allows the temperature gradient from the guard heater to the attachment to the PCB, while there is an isothermal zone under the die. The ceramic cantilever based micro-heater topology is presented in Fig. 6.2, where the dimensions of the isothermal area are $5\times5\ mm^2$.

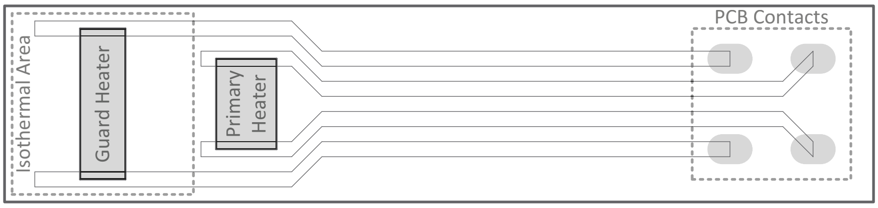


Figure 6.2: The Ceramic Cantilever Based Micro-Heater Topology.

The cantilever is manufactured using a hybrid thick film on a 0.635 mm thick *Alumina* substrate. The tracks are printed with *Silver-Palladium*. The pads for soldering are printed with Ag-Pd as well. The contact pads for the resistor are printed with *Silver*. The heating elements, essentially resistive heaters, are printed with a PTC (*Positive Temperature Coefficient*) paste. A layer of protective glass coating is printed over the tracks and resistors. After printing, each layer was fired in a belt furnace at 850°C with a ten minutes time at the peak temperature.

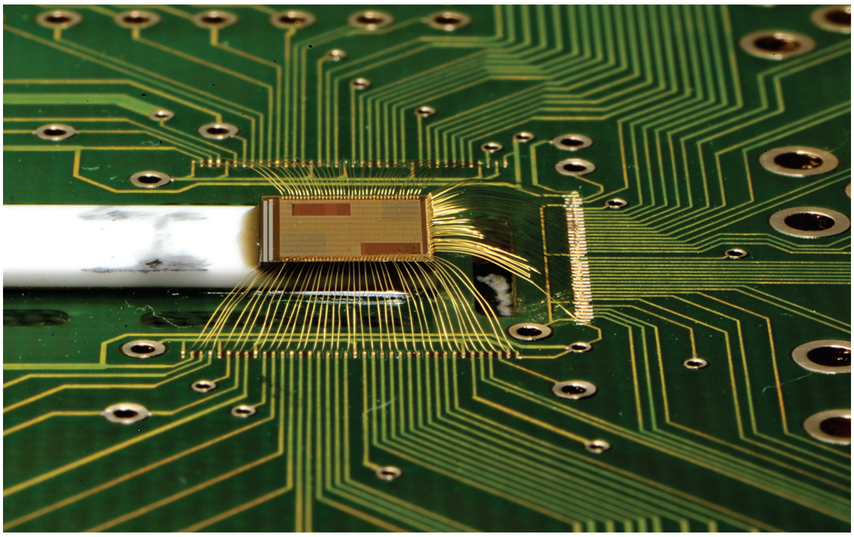


Figure 6.3: The SRAM Test Chip Mounted on the Micro-Heater.

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[1] The micro-heater design and implementation is done by the *Laboratory of Microengineering for Manufacturing* (LPM) at *Swiss Federal Institute of Technology Lausanne* (EPFL). Also, closed-loop die temperature regulation implementation and high temperature measurements are done in collaboration with this group.

Once fabricated, the micro-heater is mounted directly on the PCB to make both a mechanical attachment and electrical contacts for the heaters. After this step, the electrical connections in between the DUT and the PCB landings are made using the COB technique. Basically, the wirebonds are directly bonded from the pads of the chip to the PCB landings. The only drawback of the micro-heater test-bench is that it allows connections to three sides of the die. One side is always prohibited for the COB technique having that is is used for the cantilever attach. The cantilever based micro-heater implementation is presented in Fig. 6.3. This test-bench was used for the high temperature measurements performed on the Latch based SRAM module fabricated in 0.18μm SOI process, which has been earlier described in Chapter 3.

6.2.1 The Bare Die Verification

The COB is a very conservative technique, comparing to the standard chip packaging. The standard approach allows flexibility for the DUT to be plugged into the PCB mounted sockets. Eventually, the DUT can be unplugged and replaced by another chip if needed. On contrary to that, the COB technique does not allow any replacements of the DUT and once implemented, the DUT is permanently attached to the PCB. Taking it into account, we must be certain of the DUT functionality.

That is why the wafer-level verification is needed for selecting the functional bare dies. A standard wafer-level bare die verification is performed using a probe-card and a probe station which provides mechanical support for the experiment. The probe-card lands on the wafer surface, so that its probes establish electrical contacts with the pads. This configuration allows us verify the die functionality and it is electrically equivalent to the test-bench which is used for the further measurements and tests. The probe-card implementation is presented in Fig. 6.4. This probe-card was used for the wafer-level verification of the Firebird SoC, which has been earlier described in Chapter 4.

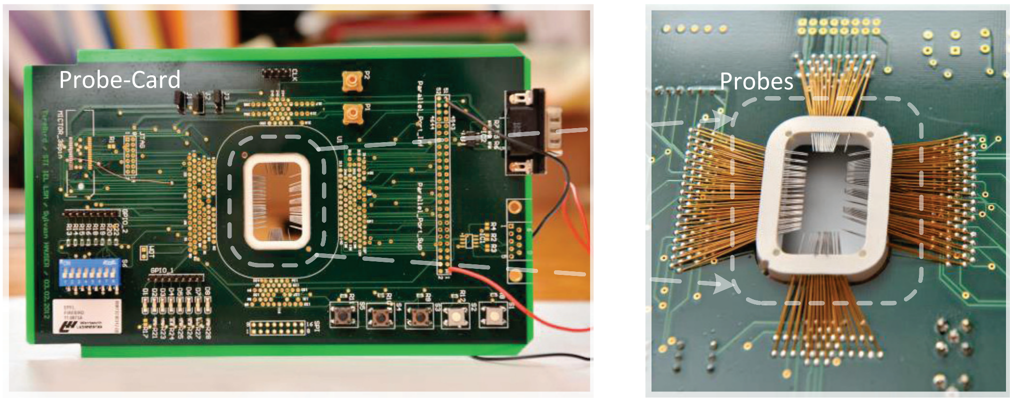

Figure 6.4: The Probe-Card Used for Firebird SoC Bare Die Verification.

6.3 Closed-Loop Die Temperature Regulation

For the die temperature regulation of the DUT mounted on top of the cantilever based micro-heater, we designed a control application in LabVIEW. The main operating principle consists of applying a voltage across the resistive micro-heaters for dissipating the thermal energy. The dissipated heat is then transferred to the DUT. To obtain the closed-loop regulation, the micro-heaters temperature is measured and the control voltages are updated accordingly using a PID (*Proportional-Integral-Derivative*) controller.

The LabVIEW control application manipulates with a dual-output power supply, *Agilent Technologies* E3631A, that is capable of measuring the current and voltage supplied to the two heaters independently. This information is used to calculate the thermally-dependent resistance, R_T, of the two heaters. Taking into account the micro-heater resistances, R_0, at room temperature of 25°C, the micro-heater temperature, $T_{\mu H}$, could be retrieved from the following equation:

$$R_T = R_0 \times (1 + \alpha T_{\mu H}) \Rightarrow T_{\mu H} = \frac{R_T - R_0}{\alpha R_0} \tag{6.1}$$

where α is the TCR (*Temperature Coefficient of Resistance*) and it is equal to 3000 $ppm/°C$. Based on this temperature calculation, both heaters are controlled using proportional regulation. The primary heater should follow the desired temperature set by the LabVIEW control application and the guard heater controller is programmed to follow the measured temperature of the primary heater, providing the isothermal conditions for the DUT. The closed-loop regulation algorithm, implemented by LabVIEW control application, is presented in Fig. 6.5.

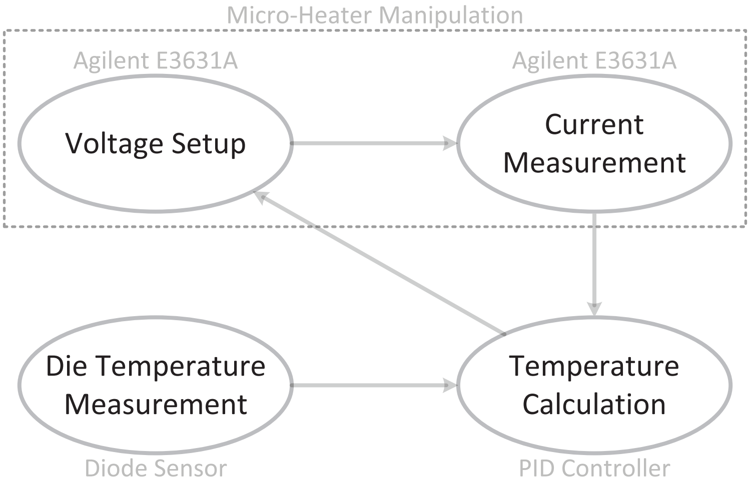

Figure 6.5: The Closed-Loop Regulation Algorithm.

In parallel to the micro-heater temperature regulation, the die temperature is measured using on-chip diode sensor. We have to be sure that the die temperatures follow micro-heaters temperatures defined by the LabVIEW control application. The die temperature measurements are compulsory for this sort of high temperature experiments, having that it reveals eventual existence of heat sinks in between the micro-heater and the DUT.

6.3.1 The Diode Sensor for Die Temperature Measurements

On-chip diode sensors found their application in the processors long time ago. It has been reported that the ADSP-214xx SHARC processor from *Analog Devices*, the PowerPC970MP processor from *IBM Corporation*, the Pentium Core Duo E2000 processor from *Intel Corporation* [97], incorporate an on-chip thermal diode for die temperature measurements.

The die temperature extraction from the diode equations is done analytically using two diode operating points ($I_{AC1,2}$,$V_{AC1,2}$). In order to derive temperature dependence, let us recall on the diode equations, previously presented in Chapter 2:

$$I_{AC} = I_S \times exp\left(\frac{V_{AC}}{nV_t}\right) \tag{6.2}$$

where I_S is the reverse bias saturation current, n is ideality factor which represents an empirical and process-dependent constant, typically equal to $n \approx 1$, and V_t is the thermal voltage which contains the die temperature value:

$$V_t = \frac{kT}{q} \tag{6.3}$$

where k is Boltzmann's constant and q is elementary charge. Thus, in these equations, all the variables are know apart from the reverse bias saturation current I_S. From the physical point of view, the I_S variable strongly depends on the process parameters and variations. Its value could not be easily calculated and must be measured, what makes it very impractical for use. However, from the analytical point of view, the I_S variable could be eliminated from equation if we introduce two diode operating points, defined by ($I_{AC1,2}$,$V_{AC1,2}$). The I_S variable elimination is possible by dividing the two diode equations and it results by the following relation:

$$\frac{I_{AC2}}{I_{AC1}} = exp\left(\frac{V_{AC2} - V_{AC1}}{nV_t}\right) \tag{6.4}$$

where all the variables are known and could be used for the die temperature extraction. The die temperature value is embedded into the thermal voltage, V_t, and we have to manipulate the previous equation in order to get it.

The thermal voltage V_t value is determined by applying the *Natural logarithm* to the previous equation:

$$\ln\left(\frac{I_{AC2}}{I_{AC1}}\right) = \frac{V_{AC2} - V_{AC1}}{nV_t} \Rightarrow V_t = \frac{V_{AC2} - V_{AC1}}{n\ln\left(\frac{I_{AC2}}{I_{AC1}}\right)} \tag{6.5}$$

where the die temperature could be simply extracted from the thermal voltage V_t and determined by the final equation:

$$T = \frac{q\,(V_{AC2} - V_{AC1})}{k\ln\left(\frac{I_{AC2}}{I_{AC1}}\right)} \tag{6.6}$$

where the ideality factor is approximated by $n \approx 1$. This equation provides the die temperature value based on two diode operating points measurements. The two diode operating points are measured using the *Agilent Technologies* E3631A power supply and the die temperature is calculated using the LabVIEW control application. The die temperature measurements, using the on-chip diode sensor, are presented in Fig. 6.6.

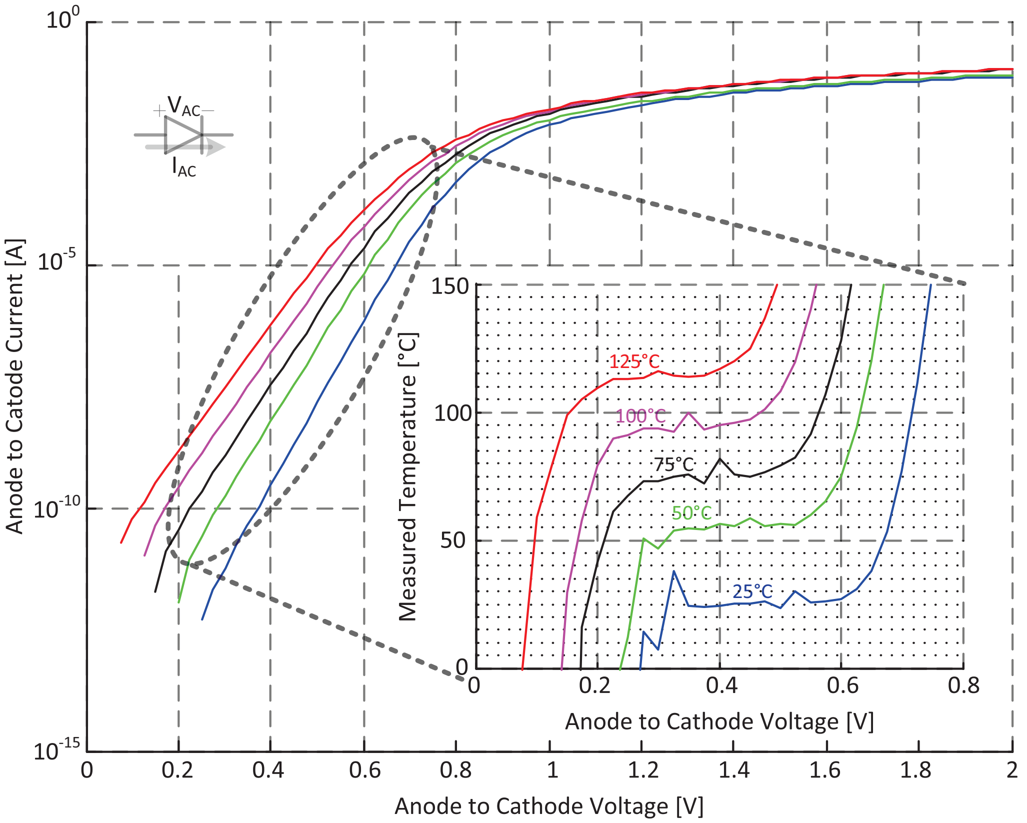

Figure 6.6: The Die Temperature Measurements Using on-Chip Diode Sensor.

As it could be observed for the *Anode* to *Cathode* voltage V_{AC}, the temperature measurements are preferable in the region in between 0.25 V and 0.55 V. Accordingly, for the *Anode* to *Cathode* current I_{AC}, the preferable region for measurements is in between $\approx 1\ nA$ and $\approx 100\ \mu A$. Finally, the maximum measurement error is approximately $T_{ERR} \approx 5°$C.

6.4 Measurement Results

The operation principles of the PID controller, implemented in the LabVIEW control application, are presented in Fig. 6.7.

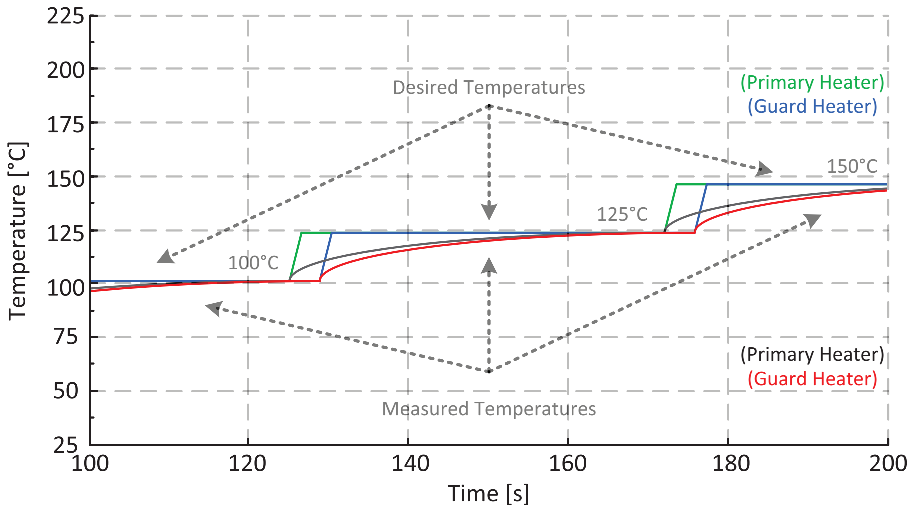

Figure 6.7: The Micro-Heater Temperatures Regulation Using the PID Controller.

The measurement results, presented in the previous figure, are taken as a snapshot from the LabVIEW control application. The temperatures plotted in *green* and *blue* are specified in the control application by user, for the primary and guard heaters, respectively. As it could be observed, the desired temperature of the primary heater is each time set up earlier then for the guard heater. The reason for this is that we want first to dissipate the heat from the main heating element, and then to perform a fine temperature matching using the secondary heating element [98].

Further, the temperatures plotted in *black* and *red* are measured by control application, for the primary and guard heaters, respectively. Hence, in order to perform the closed-loop regulation, we must measure the variable we are controlling and compare it to the desired value. It could be observed that both regulated temperatures converge to desired value and, more importantly, that occurs for a very short time interval. Typically, the heating time interval is measured to be $t_{HEAT} \approx 60\ s$ for the temperature difference of 25°C. It could be also observed that both heating elements achieve the desired temperature at the same time. It comes from the PID controller characteristics and guarantees faster temperature regulation.

Finally, the heat transfer from the cantilever to the DUT is validated using the *FLIR Systems* SC655 infra red camera. An image of the micro-heater test-bench at 250°C is presented in Fig. 6.8. It could be observed that there is an uniform distribution of the heat over the surface of the die that we are measuring. On contrary to that, there is a desirable gradient of the heat from the die to the PCB attachment. This measurement result strongly confirms our design expectations of localized heat transfer to the DUT. This test-bench configuration allows placing standard electronic components in the remaining space on the PCB and this is the main advantage comparing to the conventional high temperature ovens.

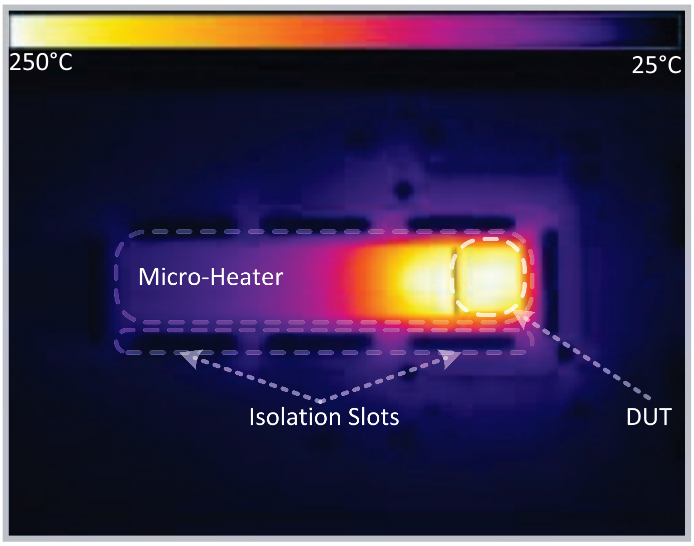

Figure 6.8: The Test-Bench Validation Using an Infra Red Camera.

6.4.1 The Chip-On-Board Implementation Drawbacks

Obtaining sufficient quality of the COB connectivity is very challenging and it requires Ag/Cu PCB landings to be properly printed. If this requirement is not satisfied, assuming inaccuracies at shapes or metal thicknesses, there is high probability that the bonding machine operation will crack it, making an irreversible damage. Typical PCB fabrication failures are presented in the Fig. 6.9.

The thickness of cantilever is as important as the PCB manufacturing quality. Higher the DUT is placed with respect to the PCB, longer the wirebonds. Long wirebonds introduce serial resistance and inductance, which are non desired parasitics [99]. Also, if the cantilever is too high, bonding machine can face severe issues and the bonding might not be possible at all. These are, essentially, the main drawbacks of the COB implementations. However, despite the anticipated risk introduced by the COB technique, we managed to obtain a very high yield in our low-cost high-precision thermally-controlled test-bench designs.

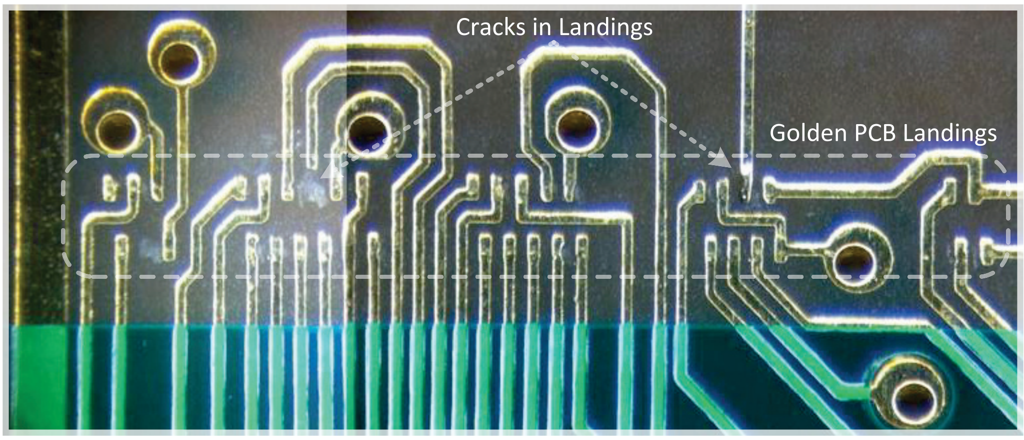

Figure 6.9: Cracks in the Golden PCB Landings.

A successful COB implementation is presented in Fig. 6.10. This test-bench was used for the room temperature verification of the Firebird SoC, which has been earlier described in Chapter 4. This COB implementation involves as much as 256 successfully soldered wirebonds.

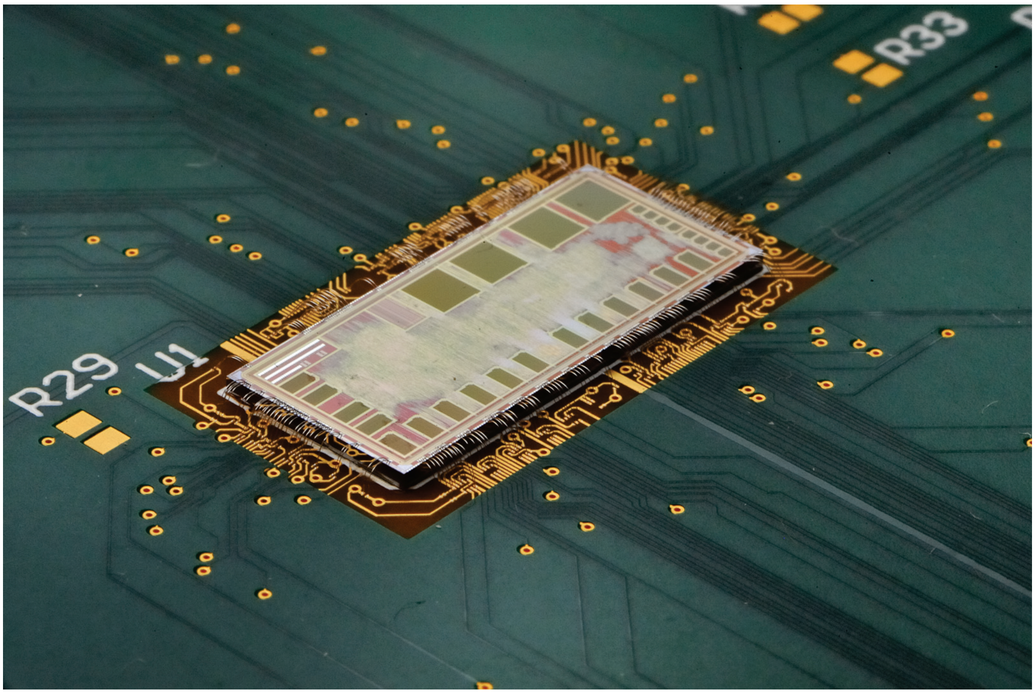

Figure 6.10: The Firebird SoC COB Test-Bench.

6.5 Conclusion

In this chapter, we introduce a novel low-cost high-precision thermally-controlled test-bench design for high temperature experiments. The proposed concept relies on the cantilever based micro-heater implementation for providing mechanical support and heat transfer to the design under tests. A fully-automated LabVIEW control application is developed to regulate micro-heater temperatures using a PID controller. In parallel to that, the die temperature is measured using the diode based sensor, guaranteeing that desired temperature is achieved.

The cantilever based micro-heater test-bench is capable of reaching 250°C, what has been verified using an infra red camera. We report a typical heating time interval of $t_{HEAT} \approx 60\ s$ for the temperature difference of 25°C. This result indicate much better performance comparing to its expensive high temperature test-bench competitors.

7 Conclusions

In this thesis we presented a novel, fully-digital approach in designing Systems-on-Chip for operation at high temperatures. We covered by this work the design, implementation, fabrication and high temperature measurements of SRAM, microcontroller, temperature sensor and data converter, which are the essential parts of state-of-the-art SoC. We may conclude that the main contribution of this thesis is delivering a set of design techniques for improving reliability of the SoC for operation at high temperatures.

The first major contribution of this thesis is an integral failure analysis of the conventional 6T SRAM cells, which takes both the operating temperature and power supply variations into account. We contribute even more significantly by introducing a novel fully-digital Latch based SRAM module that is robust to thermally-caused failure mechanisms at elevated temperatures.

The second major contribution comes from designing a SoC for reliable operation at high temperatures. We proposed a PowerPC based SoC, customized by using the dynamically reconfigurable clock frequency, exhaustive clock gating, and electromigration-resistant power distribution network. These design decisions preserved system performance despite the increased static leakage current, reduced carrier mobility, and decreased driving strengths of the MOS transistors at elevated temperatures.

The third and final major contribution of this thesis is a novel time-domain design technique which exploits the adaptive body-biasing and a single clock cycle Time-to-Digital conversion. We revealed its strengths in processing digital signals and demonstrated, by the digital temperature sensor and Pulse based Flash ADC implementations, its eligibility for applications which assume operation at high temperatures.

Finally, this thesis provided a set of custom micro-heaters based measurement and test techniques that could be used for high temperature experiments. As such, this thesis provides integral study on reliable design, implementation and characterization of the SoC for operation as high temperatures.

7.1 Future Work

The future work in achieving even more reliable SoC for operation at high temperatures would involve integration of all the previously mentioned design techniques at the same time. We already explained various concepts of improving reliability and preserving performance at elevated temperature. These concepts could be classified in the following levels, using the down-top approach:

• **Fabrication process level**: Low leakage currents and high driving strengths are qualifying the SOI process as the right choice for high temperature applications. Next generations of the wide band gap semiconductors, including the SiC and GaN, are very promising, but presently they cannot compete to the commercial SOI processes.

• **VLSI design level**: First of all, the electromigration-resistant power distribution network must be designed to ensure reliable operation despite the increased total power consumption at elevated temperatures. Further, the adaptive body-biasing should be applied to compensate thermally-caused threshold voltage variations. Finally, the operation principles which process digital signals should be often used. For instance, the Time-to-Digital conversion is a typical example of the fully-digital technique that reliably operates at high temperatures. Also, the 6T SRAM cell substitution by a latch is the same sort of fully-digital customization.

• **System architecture level**: Inherent low power processor architectures, such as the PowerPC, should be used for achieving minimal power consumptions. Further, reliable Latch based SRAM modules must be used for preserving the critical instruction code sections when the 6T SRAM module becomes useless due to the thermally-caused failures. Finally, on-chip digital temperature sensors for measuring die temperatures are needed for the thermal management of the SoC.

• **Software application level**:The software based self-test method should be compiled into the on-chip ROM module and executed when the high temperature testing and characterization is needed. More importantly, the system should be capable of dynamical clock frequency reconfiguration. Once the die temperature increases, a software routine should reduce operating frequency to the value which guaranties reliable operation.

Hence, the next generation of the Firebird SoC should implement all these hardware and software design techniques for reaching higher reliability. Besides, the silicon die, integrating the SoC, should be supported by the appropriate packaging, assuming the COB technique implemented on the LTCC substrate.

7.2 Outlook

At the time of writing this thesis, the high temperature product lines are being introduced by several companies. Currently the main application of these highly reliable products is downhole oil drilling, as could be seen in the proceedings of the HiTEN (*High Temperature Electronics Network*) conference held in Oxford, UK in 2013 [1]. However, we may also see increased interest in the modern aerospace industry, requiring highly reliable electronic components for the next generation aircraft.

We also believe that the next generation electric cars will require high temperature electronic components for motor control application. The premium electric vehicle manufacturer *Tesla Motors* could be seen as the pioneer in integrating the high temperature electronic components in their state-of-the-art fully-electric cars. In parallel with the applications in electric vehicles, we may think of the drone manufactures as a new consumer of the high temperature electronic components. Unlike the aircraft, drones do not have humans on board. It reduces required reliability levels for electronic components to be integrated into drones, comparing to the modern aircraft. The drone manufacturers may eventually become the biggest consumer of the high temperature electronic components.

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- PhD in Microelectronics
- Broad knowledge of Digital systems
- Dynamic team player with excellent social skills

Profile

ASIC designer

Work experience

Employer	**Samsung Electronics, Gyeonggi-do, Hwaseong, South Korea (July - September 2013)**
Position held	Reliability engineer, Analog Team, Flash Design Team, Memory Division
Project title	*"Reliable Digital Temperature Sensor for Flash Memory Modules"*
Main contributions	Digital CMOS IC design, Thermal caused failure analysis and Reliability engineering
Employer	**CSEM, Jaquet-Droz 1, Neuchatel, Switzerland (September 2009 - March 2010)**
Position held	RTL design engineer, SoC Section, Microelectronics Department
Project title	*"The Data Processing Unit for the icyflex2 Processor"*
Main contributions	RTL Design, Verification and Logic Synthesis

Education

	PhD in Microelectronics (April 2010 – October 2014)
Principal subjects	• Leakage reduction techniques in standard SOI and Bulk CMOS processes • Reliable implementations of digital temperature sensors and A/D converters • Latch SRAM and SoC design for reliable operation at high temperatures
Digital CMOS ICs	• 0.18µm IBM 7RFSOI CMOS: 6T and Latch SRAM • 0.35µm XFAB XA035 CMOS: 64bit PowerPC, 64kB SRAM, 32kB Cache SoC • 0.18µm UMC CMOS: 300fJ/conversion 5bit 50MSample Flash ADC
Teaching Assistant	VHDL, EDA and VLSI Design
School	STI School, Swiss Federal Institute of Technology Lausanne, EPFL
	MSc in Microelectronics (September 2008 – March 2010)
Principal subjects	Analog, Embedded systems and VLSI design, Hardware modelling and Verification
School	Swiss Federal Institute of Technology Lausanne, EPFL
	BSc in Electrical Engineering (October 2004 – August 2008)
Principal subjects	Analog and Digital electronics
School	Faculty of Electrical Engineering, University of Belgrade, ETF

Skills overview

Trainings	"Venture Challenge" (Venture Lab, 2013), "High Performance Data Converters", (MEAD, 2012)
Software	Linux (tcl, gcc), MacOS, Latex, Photoshop CS, Visio
EAD tools	ModelSim, Synopsis DC, Cadence Virtuoso, Cadence SoC Encounter, Xilinx ISE, LabView

Languages

English (fluent), French (independent), Serbian (native)

Personal interests

Social	"Serbian Young Talents Foundation Member" (2009), "Freedom Journalist" (2002)
Arts	Rock music, Photography, Theatre.
Sports	Basketball coach and arbiter, (American) Football and Soccer player, Snowboarder

Personal information

29 years old, Single, Serbian

Radisav Cojbasic – Cirriculum Vitae – Version: September 2014.